Attorney Docket No. 0756-0945

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 2677
Hisato Shinohara et al.	)	Examiner: Marianne L. Padgett
Serial No. 08/169,127	)	Group Art Unit: 1792
Filed: December 20, 1993	)	
For: LASER IRRADIATION METHOD	)	
	)	
	)	

RESPONSE TO NOTIFICATIONS OF NON-COMPLIANT APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The *Order Returning Undocketed Appeal to Examiner* mailed June 3, 2009 (signed by Gloria J. Henderson, Review Team Paralegal, hereinafter "the *Order*" or "the Board's *Order*"), the *Notification of Non-Compliant Appeal Brief* mailed June 6, 2009 (signed by Bridget C. Monroe, Patent Appeals Center Specialist, hereinafter "the first *Notification*"), and the *Notification of Non-Compliant Appeal Brief* mailed June 15, 2009 (signed by Primary Examiner Marianne L. Padgett, hereinafter "the second *Notification*" or "the Examiner's second *Notification*"), have been received and their contents carefully noted. This response is filed within one month of the mailing date of the first *Notification*, and therefore is believed to be timely without extension of time. Accordingly, the Appellant respectfully submits that this response is being timely filed.

At issue is whether, consistent with the Board's *Order* after an *Examiner's Answer* but Before the Board's Decision, the Examiner should follow such *Order* directing the Examiner to direct the Appellant to provide copies of U.S. Patent No. 7,416,907 to Yamazaki and U.S. Patent No. 7,381,599 to Konuma. As noted in MPEP

§ 1206, "An amendment, affidavit or other evidence received after jurisdiction has passed to the Board should not be considered by the examiner unless remanded or returned by the Board for such purpose. See MPEP § 1210 and § 1211.02" (emphasis added). As noted in MPEP § 1210, titled "Actions Subsequent to Examiner's Answer but Before Board's Decision" and in 37 CFR § 41.35, "If, after receipt and review of the proceeding, the Board determines that the file is not complete or is not in compliance with the requirements of this subpart, the Board may relinquish jurisdiction to the examiner or take other appropriate action to permit completion of the file." The Board has determined that the file is not complete and has requested that copies of Yamazaki and Konuma be submitted to the record. Also, presumably, the Board is well aware of the new evidence rule and did not issue such objection. Therefore, the Appellant respectfully requests that the Examiner comply with the Board's explicit request. In response to this request, the Appellant submits herewith Yamazaki and Konuma, which are cited on page 24 of the *Appeal Brief* filed November 18, 2008, and noted in the Evidence Appendix at page 43 of the same.

Also, apparently contrary to the *Order*, after issuance of an *Examiner's Answer*, the Examiner raises a new issue questioning whether such citations are "impermissible new evidence." The Appellant respectfully submits that Examiner Padgett's refusal to accept the citation of Yamazaki and Konuma is particularly egregious in light of the fact that these citations are provided in direct response to Examiner Padgett's own concerns, namely the Examiner's request for an explanation of the criticality and meaning of the term "peripheral circuit," raised by the Examiner during a personal interview conducted during prosecution on June 6, 2007. The meaning of "peripheral circuit" is pertinent to the question of whether claims 71, 76, 164 and 165 are properly rejected under the doctrine of obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent No. 6,261,856 to Shinohara. To date, the Examiner apparently ignores the meaning of the term "peripheral circuit" when ascertaining the scope of claims 71, 76, 164 and 165, and the Appellant has noted that the claims of

Shinohara do not teach or suggest at least this feature. Although the Appellant has provided citations to the present specification and drawings to support the Appellant's position on the matter, the Appellant believes that the Board and the general public would be further served by review of Yamazaki and Konuma. To the extent that the Examiner is permitted to ignore the Board's *Order* and raise a new issue after issuance of the *Examiner's Answer*, the Appellant requests that the Examiner admit these citations to assist the Board in determining the criticality and meaning of the term "peripheral circuit" in deciding the question of whether claims 71, 76, 164 and 165 are properly rejected under the doctrine of obviousness-type double patenting as being unpatentable over claims 1-39 of Shinohara '856.

Further, regardless of whether Yamazaki and Konuma are admitted or not, the Appellant respectfully submits that the present specification literally supports the recitation of "peripheral circuit," for example, at page 11, lines 3-11, which discloses the following (emphasis added):

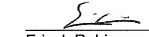
> Referring to FIG., 7(B), the semiconductor layer 52 and the insulating layer 59 are simultaneously patterned by a suitable etching method in order to form a plurality of semiconductor islands 58 covered by the insulating layer. The islands are arranged in rows and columns as shown in FIG. 8. For clarification, only 5×5 islands are shown in FIG. 8. However, in practice, 480×640 or 960×1920 islands may be formed on one substrate. It is also possible to form other semiconductor islands on the same substrate in order to form a driver circuit or peripheral circuit for driving the pixel TFTs.

The Appellant further respectfully submits that one of ordinary skill in the art, upon review of the present specification, including the above-referenced portions, would readily understand the meaning of "a peripheral circuit" as being, for example, a circuit for driving pixel TFTs that is peripheral to the pixel TFTs. In other words, one of ordinary skill in the art at the time of the present invention understands that a peripheral circuit is not just a driver circuit, but it is a circuit that is located in a peripheral area of the device, i.e. outside the display or pixel area of a device.

Accordingly, the Appellant respectfully requests that the attached copies of Yamazaki and Konuma be provided to the Board in response to the Board's *Order* and the first *Notification*. Also, the Appellant respectfully requests that the Examiner's assertion in the second *Notification* that Yamazaki and Konuma are "impermissible new evidence" be reconsidered and withdrawn or suspended in light of the Board's direction in the aforementioned *Order* and the Appellant's belief that the Board and the general public would be further served by review of Yamazaki and Konuma in the present matter.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance or appeal, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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US007381599B2

(12) **United States Patent**
Konuma et al.

(10) **Patent No.: US 7,381,599 B2**
(45) **Date of Patent: Jun. 3, 2008**

(54) **SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME**

(75) Inventors: **Toshimitsu Konuma**, Atsugi (JP); **Akira Sugawara**, Atsugi (JP); **Yukiko Uehara**, Atsugi (JP); **Hongyong Zhang**, Yamato (JP); **Atsunori Suzuki**, Kawasaki (JP); **Hideto Ohnuma**, Atsugi (JP); **Naoaki Yamaguchi**, Yokohama (JP); **Hideomi Suzawa**, Atsugi (JP); **Hideki Uochi**, Atsugi (JP); **Yasuhiko Takemura**, Atsugi (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-ken (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/064,821**

(22) Filed: **Feb. 25, 2005**

(65) **Prior Publication Data**

US 2005/0142705 A1 Jun. 30, 2005

Related U.S. Application Data

(62) Division of application No. 08/307,167, filed on Sep. 16, 1994, now Pat. No. 6,867,431.

(30) **Foreign Application Priority Data**

Sep. 20, 1993 (JP) 05-256563
Sep. 20, 1993 (JP) 05-256565
Oct. 19, 1993 (JP) 05-284287
Sep. 20, 2003 (JP) 05-256567

(51) **Int. Cl.**
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **438/163**; 438/166

(58) **Field of Classification Search** 438/166, 438/163
See application file for complete search history.

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Primary Examiner—M. Wilczewski
(74) *Attorney, Agent, or Firm*—Eric J. Robinson; Robinson Intellectual Property Law Office, P.C.

(57) **ABSTRACT**

A TFT formed on an insulating substrate source, drain and channel regions, a gate insulating film formed on at least the channel region and a gate electrode formed on the gate insulating film. Between the channel region and the drain region, a region having a higher resistivity is provided in order to reduce an Ioff current. A method for forming this structure comprises the steps of anodizing the gate electrode to form a porous anodic oxide film on the side of the gate electrode; removing a portion of the gate insulating using the porous anodic oxide film as a mask so that the gate insulating film extends beyond the gate electrode but does not completely cover the source and drain regions. Thereafter, an ion doping of one conductivity element is performed. The high resistivity region is defined under the gate insulating film.

39 Claims, 13 Drawing Sheets

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Office Action (Application No. 200510054408.8) Dated Aug. 24, 2007.

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FIG.1A

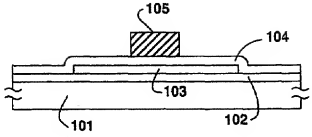


FIG.1B

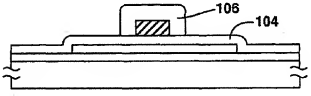


FIG.1C

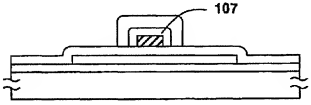


FIG.1D

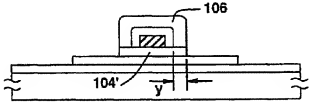


FIG.1E

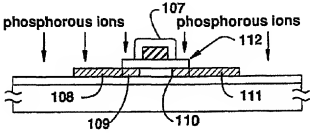


FIG.1F

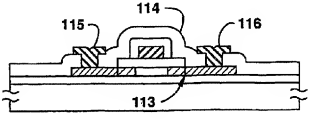


FIG.2A

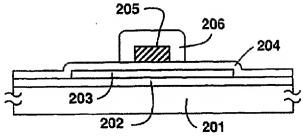


FIG.2B

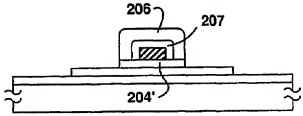


FIG.2C

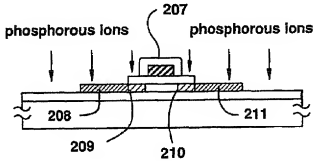


FIG.2D

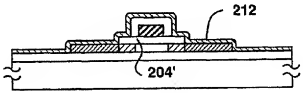


FIG.2E

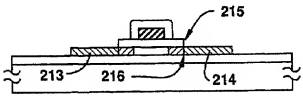


FIG.2F

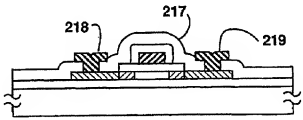


FIG.3A

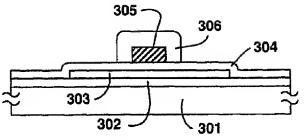


FIG.3B

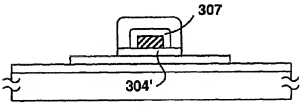


FIG.3C

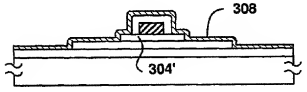


FIG.3D

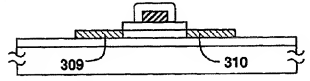


FIG.3E

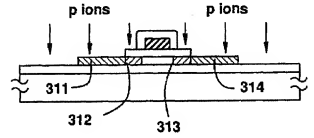


FIG.3F

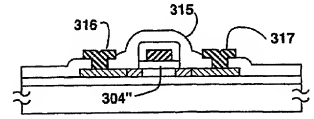


FIG.4A

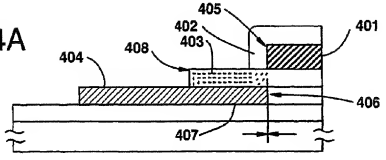


FIG.4B

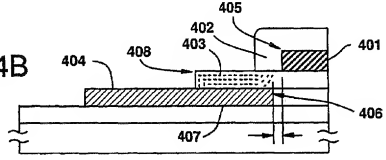


FIG.4C

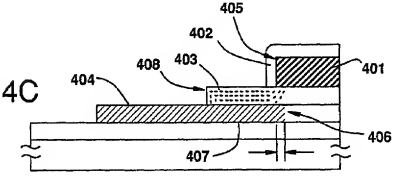


FIG.4D

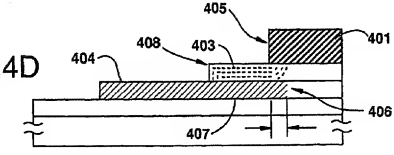


FIG.5A

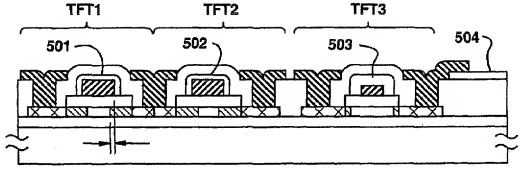


FIG.5B

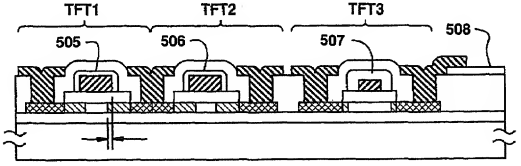


FIG.6A
PRIOR ART

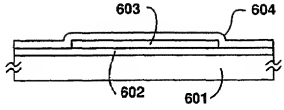


FIG.6B
PRIOR ART

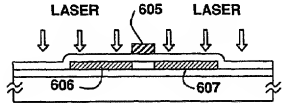


FIG.6C
PRIOR ART

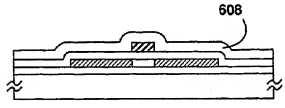


FIG.6D
PRIOR ART

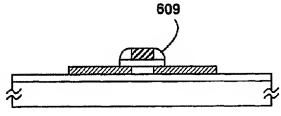


FIG.6E
PRIOR ART

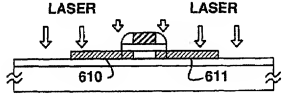


FIG.6F
PRIOR ART

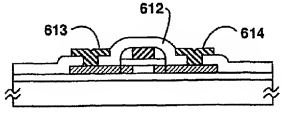


FIG.7A

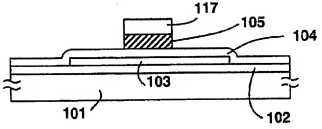


FIG.7B

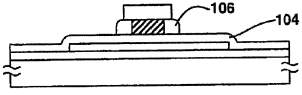


FIG.7C

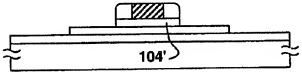


FIG.7D

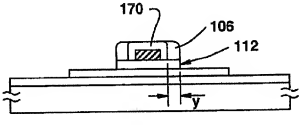


FIG.7E

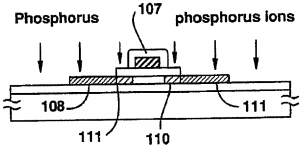


FIG.7F

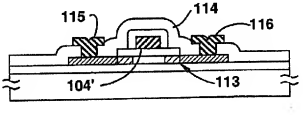


FIG.8A

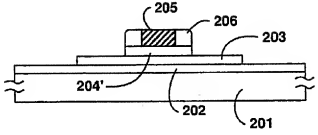


FIG.8B

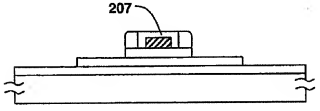


FIG.8C

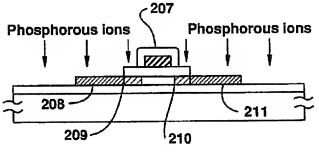


FIG.8D

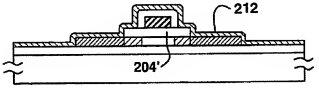


FIG.8E

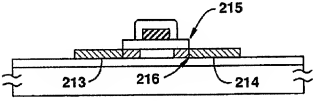


FIG.8F

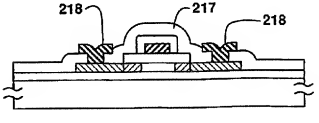


FIG.9A

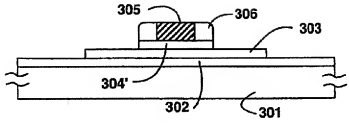


FIG.9B

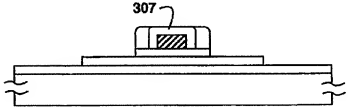


FIG.9C

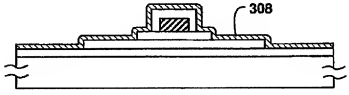


FIG.9D

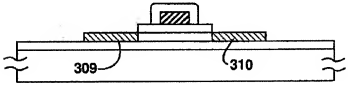


FIG.9E

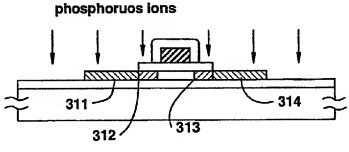


FIG.9F

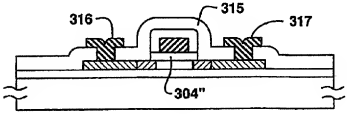


FIG.10A

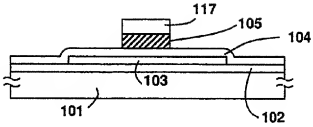


FIG.10B

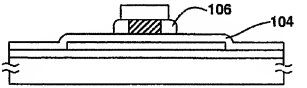


FIG.10C

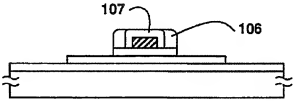


FIG.10D

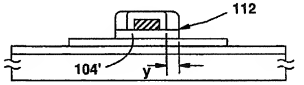


FIG.10E

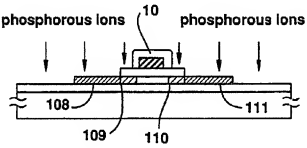


FIG.10F

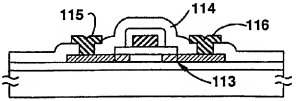


FIG.11A

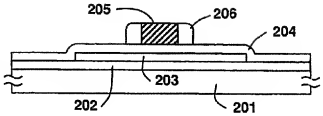


FIG.11B

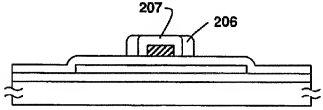


FIG.11C

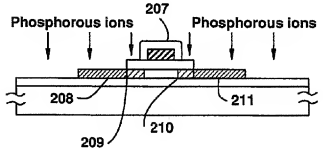


FIG.11D

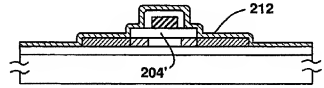


FIG.11E

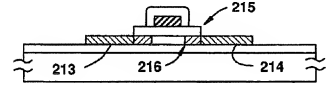


FIG.11F

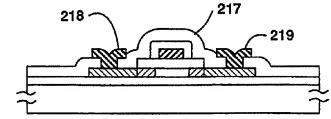


FIG.12A

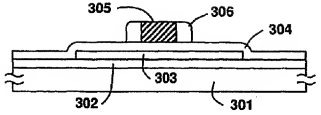


FIG.12B

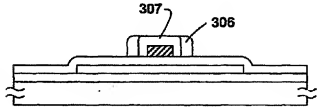


FIG.12C

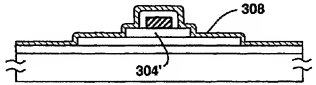


FIG.12D

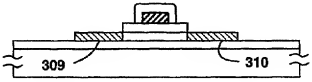


FIG.12E

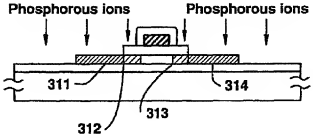


FIG.12F

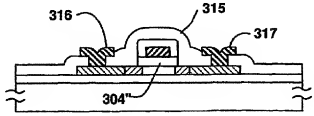


FIG.13A

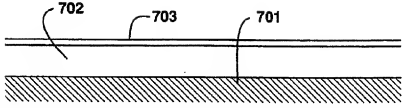


FIG.13B

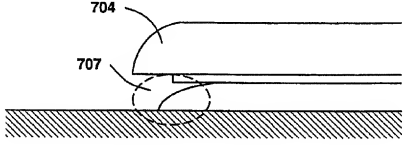


FIG.13C

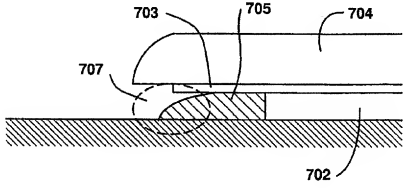
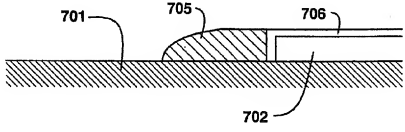


FIG.13D



SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a manufacturing method thereof, in particular, the present invention is directed to an insulated gate field effect transistor of a thin film type formed on an insulating surface which may be a surface of an insulating substrate such as glass or an insulating film such as silicon oxide formed on a silicon wafer. Specifically, the present invention is applicable to a manufacture of a TFT (thin film transistor) formed on a glass substrate of which glass transition temperature (which is also called distortion point or distortion temperature) is 750° C. or lower.

The semiconductor device manufactured in accordance with the present invention is applicable to a driving circuit for an active matrix device such as a liquid crystal display or an image sensor, or a three dimensional integrated circuit.

TFTs have been well known to drive an active matrix type liquid crystal device or an image sensor specifically, instead of amorphous TFTs having an amorphous silicon as an active layer thereof, crystalline Si TFTs have been developed in order to obtain a higher field mobility. FIGS. **6**A-**6**F are cross sections showing a manufacturing method of a TFT in accordance with a prior art.

Referring to FIG. **6**A, a basc film **602** and an active layer **603** of crystalline silicon are formed on a substrate **601**. An insulating film **604** is formed on the active layer using silicon oxide or the like.

Then, a gate electrode **605** is formed from phosphorous doped polysilicon, tantalum, titanium, aluminum, etc. With this gate electrode used as a mask, an impurity element (e.g. phosphorous or boron) is doped into the active layer **603** through an appropriate method such as ion-doping in a self-aligning manner, thereby, forming impurity regions **606** and **607** containing the impurity at a relatively lower concentration and therefore having a relatively high resistivity. These regions **606** and **607** are called a high resistivity region (HRD: High Resistivity Drain) by the present inventors hereinafter. The region of the active layer below the gate electrode which is not doped with the impurity will be a channel region. After that, the doped impurity is activated using laser or a heat source such as a flush lamp. (FIG. **6**B)

Referring to FIG. **6**C, an insulating film **608** of silicon oxide is formed through a plasma CVD or APCVD (atmospheric pressure CVD), following which an anisotropic etching is performed to leave an insulating material **609** adjacent to the side surfaces of the gate electrode as shown in FIG. **6**D.

Then, using the gate electrode **605** and the insulating material **609** as a mask, an impurity element is again added into a portion of the active layer **603** by an ion doping method or the like in a self-aligning manner, thereby, forming a pair of impurity regions **610** and **611** containing the impurity element at a higher concentration and having a lower resistivity. Then, the impurity element is again activated using laser or flush lamp. (FIG. **6**E)

Finally, an inter layer insulator **612** is formed on the whole surface, in which contact holes are formed on the source and drain regions **610** and **611**. Electrode/wirings **613** and **614** are then formed through the contact holes to contact the source and drain regions. (FIG. **6**F)

The forgoing process was achieved by copying the old LDD technique for a conventional semiconductor integrate

circuit and this method has some disadvantages for a thin film process on a glass substrate as discussed below.

Initially, it is necessary to activate the added impurity element with laser or flush lamp two times. For this reason, the productivity is lowered. In the case of a conventional semiconductor circuit, the activation of an impurity can be carried out by a heat annealing at one time after completely finishing the introduction of the impurity.

However, in the case of forming TFTs on a glass substrate, the high temperature of the heat annealing tends to damage the glass substrate. Therefore, the use of laser annealing or flush lamp annealing is necessary. However, these annealing is effected on the active layer selectively, that is, the portion of the active layer below the insulating material **609** is not annealed, for example. Accordingly, the annealing step should be carried out at each time after an impurity doping is done.

Also, it is difficult to form the insulating material **609**. Generally, the insulating film **608** is as thick as 0.5 to 2 μm while the base film. **602** on the substrate is 1000-3000 Å thick. Accordingly, there is a danger that the base layer **602** is unintentionally etched and the substrate is exposed when etching the insulating film **608**. As a result, a production yield can not be increased because substrates for TFTs contain a lot of elements harmful for silicon semiconductors.

Further, it is difficult to control the thickness of the insulating material **609** accurately. The anisotropic etching is performed by a plasma dry etching such as a reactive ion etching (RIE). However, because of the use of a substrate having an insulating surface as is different from the use of a silicon substrate in a semiconductor integrated circuit, the delicate control of the plasma is difficult. Therefore, the formation of the insulating material **609** is difficult.

Since the above HRD should be made as thin as possible, the above difficulty in precisely controlling the formation of the insulating material **609** makes it difficult to mass produce the TFT with a uniform quality. Also, the necessity of performing the ion doping twice makes the process complicated.

BRIEF SUMMARY OF THE INVENTION

An object of the present invention is to solve the foregoing problems and provide a TFT having a high resistivity region (HRD) through a simplified process. Here, the HRD includes not only a region which contains an impurity at a relatively low concentration and has a relatively high resistivity, but also includes a region which has a relatively high resistivity because of an addition of an element for preventing the activation of the dopant impurity even though the concentration of the dopant impurity is relatively high. Examples of such element are carbon, oxygen and nitrogen.

In accordance with the present invention, a surface of a gate electrode is oxidized and this oxide layer is used to define the high resistivity region. The oxide layer is formed, for example, by anodic oxidation. The use of the anodic oxidation to form the oxide layer is advantageous as compared with the anisotropic etching mentioned above because the thickness of the anodic oxide layer can be precisely controlled and can be formed as thin as 1000 Å or less and as thick as 5000 Å or more with an excellent uniformity.

Further, it is another feature of the present invention that there are two kinds of anodic oxide in the above mentioned anodic oxide layer. One is called a barrier type anodic oxide and the other is called a porous type anodic oxide. The porous anodic oxide layer can be formed when using an acid electrolyte. A pH of the electrolyte is lower than 2.0, for

example, 0.8-1.1 in the case of using an oxalic acid aqueous solution. Because of the strong acidness, the metal film is dissolved during the anodization and the resultant anodic oxide becomes porous. The resistance of such a film is very low so that the thickness of the film can be easily increased. On the other hand, the barrier type anodic oxide is formed using a weaker acid or approximately neutral electrolyte. Since the metal is not dissolved, the resultant anodic oxide becomes dense and highly insulating. An appropriate range of pH of the electrolyte for forming the barrier type anodic oxide is higher than 2.0, preferably, higher than 3, for example, between 6.8 and 7.1.

While the barrier type anodic oxide can not be etched unless a hydrofluoric acid containing etchant is used, the porous type anodic oxide can be selectively etched with a phosphoric acid etchant, which can he used without damaging other materials constructing a TFT, for example, silicon, silicon oxide. Also, both of the barrier type anodic oxide and the porous type anodic oxide are hardly etched by dry etching. In particular, both types of the anodic oxides have a sufficiently high selection ratio of etching with respect to silicon oxide.

The foregoing features of the present invention facilitate the manufacture of a TFT having a HRD.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**A-**1**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 1 of the invention;

FIGS. **2**A-**2**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 2 of the invention;

FIGS. **3**A-**3**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 3 of the invention;

FIGS. **4**A-**4**D are enlarged views of a part of a TFT in accordance with the present invention;

FIGS. **5**A and **5**B show a circuit substrate for an active matrix device which employs the TFTs in accordance with the present invention;

FIGS. **6**A to **6**F are cross sectional views showing a manufacturing method of a TFT in the prior art;

FIGS. **7**A-**7**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 4 of the invention;

FIGS. **8**A-**8**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 5 of the invention;

FIGS. **9**A-**9**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 6 of the invention;

FIGS. **10**A-**10**F are cross sectional views showing a manufacturing method of a TFT in accordauce with the Example 7 of the invention;

FIGS. **11**A-**11**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 8 of the invention;

FIGS. **12**A-**12**F are cross sectional views showing a manufacturing method of a TFT in accordance with the Example 9 of the invention; and

FIGS. **13**A-**13**D are cross sectional views showing an anodic oxidation process in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **1**A, provided on a substrate **101** is a base insulating film **102**. An active layer **103** comprising a crystalline silicon semiconductor is formed on the base insulating film **102**. In this invention, "crystalline semiconductor" includes single crystalline, polycrystalline or semi-amorphous semiconductor, in which crystal components are contained at least partly. Further, an insulating film **104** comprising silicon oxide or the like is formed, covering the active layer **103**.

Further, on the insulating film **104**, a film comprising an anodizable material is formed. Examples of the anodizable material is aluminum, tantalum, titanium, silicon, etc. These materials can be used singly or in a multilayer form using two or more of them. For example, it is possible to use a double layer structure in which titanium silicide is formed on aluminum, or aluminum is formed on a titanium nitride. The thickness of each layer may be determined in accordance with a required device property. Subsequently, the film is patterned or etched to form a gate electrode **105**.

Then, referring to FIG. **1**B, the gate electrode **105** is anodized by supplying an electric current thereto in an electrolyte to form a porous anodic oxide **106** on the upper and side surfaces of the gate electrode. As the electrolyte for this anodic oxidation, an acid aqueous solution containing citric acid, oxalic acid, phosphoric acid, chromic acid, or sulfuri c acid at 3-20% is used. The applied voltage is 10-30 V and the thickness is 0.5 μm or more. Because of the use of an acid solution, the metal such as aluminum is dissolved during anodization and the resulted anodic oxidation film becomes porous. Also, because of the porous structure, the resistance of the oxide film is very low so that the thickness thereof can be increased with a relatively low voltage. The same applies to the use of an alkaline solution when the metal is amphoteric.

Referring to FIG. 1D, the insulating film **104** is etched by dry etching or wet etching with the anodic oxide film **106** used as a mask. The etching may be continued until the surface of the active layer is exposed or may he stopped before the surface of the active layer is exposed. However, it is preferable to continue the etching until the surface of the active layer is exposed in view of a productivity, production yield, and uniformity. The portion of the insulating film **104** under the gate electrode **105** and the anodic oxide film **106** remains as a gate insulating film **104'**. When using aluminum, tantalum or titanium as a main component of the gate electrode while the gate insulating film **104** comprises silicon oxide, it is possible to use a fluorine containing etchant such as NF_3 and SF_6 for a dry etching. In this case, the insulating film **104** is etched quickly while the etching rate of aluminum oxide, tantalum oxide and titanium oxide is enough small so that the selective etching of the insulating film **104** can be done.

Also, iu the case of using a wet etching, it is possible to use a hydrofluoric acid containing etchant such as a 1/100 hydrofluoric acid. In this case, the silicon oxide insulating film **104** can also be selectively etched hecause the etching rate of the oxide of the aluminum, tantalum, and titanium is enough small.

After etching the insulating film **104**, the anodic oxide film **106** is removed. As an etchant, a solution containing phosphoric acid may be used. For example, a mixed acid of a phosphoric acid, an acetic acid, and a nitric acid is desirahle. However, when using aluminum as a gate electrode, the gate electrode is also etched by the etchant. In

accordance with the present invention, this problem is solved by the provision of a barrier type anodic oxide film **107** between the gate electrode and the anodic oxide **106** as shown in FIG. 1C.

The anodic oxide film **107** can be formed by applying an electric current to the gate electrode after the formation of the anodic oxide **106** in an ethylene glycol solution containing a tartaric acid, boric acid, or nitric acid at 3-10%. The thickness of the anodic oxide **107** may be decided depending upon the magnitude of the voltage between the gate electrode and a counter electrode. It should be noted that the electrolyte used in this anodic oxidation is relatively neutral so that the density of the anodic oxide can be increased contrary to the use of an acid solution. Thus, a barrier type anodic oxide can be formed. The etching rate of the porous type anodic oxide is 10 times higher than that of the barrier type anodic oxide.

Accordingly, the porous anodic oxide **106** can be removed by the phosphoric acid containing etchant without damaging the gate electrode.

Since the gate insulating film **104'** is formed in a self-aligning manner with respect to the porous anodic oxide **106**, the outer edge of the gate insulating film **104'** is distant from the outer edge of the barrier type anodic oxide **107** by the distance "y" as shown in FIG. 1D. One of the advantages of the use of an anodic oxide is that this distance "y" can be decided by the thickness of the anodic oxide in a self-aligning manner.

Referring to FIG. 1E, an N-type or P-type impurity ions are accelerated into the active layer **103** to form high impurity concentration regions **108** and **111** in the portion on which the gate insulating film **104'** has been removed (or thinned) and to form low impurity concentration regions **109** and **110** on which the gate insulating film remains. The concentration of the impurity ions in the regions **109** and **110** is relatively small than that in the regions **108** and **111** because the impurity ions are introduced through the gate insulating film **104'** into the regions **109** and **110**. Also, the electrical resistance of the impurity regions **108** and **111** is lower than that of the impurity regions **109** and **110** because of the higher concentration of the added impurity. The difference in the concentration of impurity ions depends upon the thickness of the gate insulating film **104'**. Normally, the concentration in the regions **109** and **110** is smaller than that in the regions **108** and **111** by 0.5 to 3 digits.

The portion of the active layer just below the gate electrode is not doped with the impurity and can be maintained intrinsic or substantially intrinsic. Thus, a channel region is defined. After the impurity introduction, the impurity is activated by irradiating the impurity regions with a laser or a light having a strength equivalent to the laser light. This step can be finished at one step. As a result, the edge **112** of the gate insulating film **104'** is approximately aligned with the edge **113** of the high resistance region (HRD) **110** as shown in FIGS. **1**E and 1F.

As explained above, the high resistivity regions **109** and **110** can be determined in a self-aligning manner by the thickness "y" of the anodic oxide film **106** which in turn is decided by the amount of the electric current supplied to the gate electrode during the anodic oxidation step. This is much superior to the use of an insulating material adjacent to the gate electrode as shown in FIGS. **6**A-6F.

Also, the foregoing method is advantageous because the low resistivity regions and the high resistivity regions can be formed with a single impurity doping step. Also, in the prior art, there is a problem that the HRD is difficult to contact with an electrode in an ohmic contact because of its high resistivity and a drain voltage is undesirably lowered because of this resistivity while the HRD has an advantage that it is possible to avoid the occurrence of hot carriers and to increase the reliability of the device. The present invention solves these incomprehensive problems at one time and makes it possible to form the HRD having a width of 0.1 to 1 μm in a self-aligning manner and enables an ohmic contact between the electrodes and the source and drain regions.

Also, the locational relation of the boundary between the channel region and the HRD (**109** or **110**) with respect to the gate electrode can be controlled by changing the thickness of the barrier type anodic oxide **107** as explained below with reference to FIGS. **4**A-4D. For example, when using an ion doping method (also called as plasma doping) ions are introduced without being mass separated so that an approach angle of the ions is not uniform. Therefore, the ions introduced into the active layer tend to spread in a lateral direction.

FIG. **4**A shows a partial enlarged view of the TFT shown in FIG. 1E. The reference numeral **401** shows a gate electrode. The reference numeral **402** shows a barrier type anodic oxide which corresponds to the barrier type anodic oxide **107** of FIG. 1E. The reference numeral **404** shows an active layer. The thickness of the active layer is about 800 Å for example.

When the thickness of the anodic oxide **402** is approximately the same as the thickness of the active layer **404**, the edge **405** of the gate electrode is substantially aligned with the edge **406** of the HRD **407**.

When the anodic oxide layer **402** is thicker than the active layer, for example, 3000 Å, the edge **405** of the gate electrode is offset from the edge **406** of the HRD as shown in FIG. **4**B. On the other hand, when the anodic oxide **402** is relatively thin as compared with the active layer, the gate electrode overlaps the HRD as shown in FIG. **4**C. The degree of this overlapping becomes maximum when there is no anodic oxide around the gate electrode **401** as shown in FIG. 4D.

In general, the offset structure reduces a reverse direction leak current (off current) and increases the ON/OFF ratio. The offset structure is suitable for TFTs used for driving pixels of a liquid crystal device in which the leak current should be avoided as much as possible. However, there is a tendency that the anodic oxide degrades due to hot electrons occurring at the edge of the HRD and trapped by the oxide.

When the gate electrode overlaps the HRD, the above disadvantage of the degradation can be reduced and an ON current is increased. However, there is a disadvantage that a leak current increases. For this reason, the overlapping structure is suitable for TFTs provided in a peripheral circuit of a monolithic active matrix device. Accordingly, an appropriate configuration may be selected from FIGS. **4**A through **4**B depending upon the utilization thereof.

EXAMPLE 1

Referring again to FIGS. 1A-1F, a process of manufacturing a TFT will be discussed in more detail. A Corning 7059 glass substrate having a dimension 300 mm×400 mm or 100 mm×100 mm is used as the substrate **101**. A silicon oxide film having a thickness of 100-300 nm is formed on the substrate as the base film **102** through sputtering in an oxygen gas, for example. However, it is possible to use a plasma CVD using TEOS as a starting material in order to improve the productivity.

A crystalline silicon film **103** in the form of an island is formed by depositing an amorphous silicon to a thickness of

300-5000 Å, preferably, 500-1000 Å through plasma CVD or LPCVD, then crystallizing it by heating at 550-600° C. for 24 hours in a reducing atmosphere and then patterning it. Instead of a heat annealing, a laser annealing may be employed. Further, a silicon oxide film **104** is formed thereon by sputtering to a thickness of 70-150 nm.

Then, an aluminum film containing 1 weight % Si or 0.1-0.3 weight % Sc (scandium) is formed to a thickness of 1000 Å to 3 μm by electron beam evaporation or sputtering. A gate electrode **105** is formed by patterning the aluminum film as shown in FIG. **1**A.

Further, referring to FIG. **1**B, the gate electrode **105** is anodic oxidized by applying a current thereto in an electrolyte to form an anodic oxide film **106** having a thickness of 3000-6000 Å, for example 5000 Å. As the electrolyte, an acid aqueous solution of citric acid, oxalic acid, phosphoric acid, chromic acid, or sulfuric acid at 3-20% is used. The applied voltage is 10-30 V while the applied current is kept constant. In this example, an oxalic acid is used. The temperature of the electrolyte is 30° C. A voltage of 10 V is applied for 20-40 minutes. The thickness of the anodic oxide film is controlled depending upon the time for the anodic oxidation.

Subsequently, the gate electrode is subjected to a further anodic oxidation in another electrolyte comprising an ethylene glycol solution containing tartaric acid, boric acid or nitric acid at 3-10% to form a barrier type anodic oxide film **107** around the gate electrode. The temperature of the electrolyte is kept preferably lower than a room temperature, for example, 10° C., in order to improve the quality of the oxide film. The thickness of the anodic oxide film **107** is in proportion to the magnitude of the applied voltage. The applied voltage is selected from a range of 80-150 V. When the applied voltage is 150 V, the thickness becomes 2000 Å. The thickness of the anodic oxide film **107** is determined in accordance with a required configuration of the TFT as discussed with reference to FIGS. **4**A-4D, however, it would be necessary to raise the voltage to 250 V or higher to obtain an anodic oxide film having a thickness of 3000 Å or more. Since there is a danger that the TFT is damaged by such a large voltage, it is preferable to select the thickness of the anodic oxide **107** as 3000 Å or less.

Referring to FIG. **1**D, the silicon oxide film **104** is partly removed by dry etching. This etching may be either in a plasma mode of an isotropic etching or in a reactive ion etching mode of an anisotropic etching. However, the selection ratio of the silicon and the silicon oxide should be sufficiently large so that the active silicon layer should not be etched so much. Also, the anodic oxides **106** and **107** are not etched by CF_4 while the silicon oxide film **104** is selectively etched. Since the portion of the silicon oxide film **104** below the porous anodic oxide **106** is not etched, a gate insulating film **104'** remains without being etched.

Then, referring to FIG. **1**E, only the porous anodic oxide film **106** is etched by using a mixed acid of phosphoric acid, acetic acid or nitric acid at an etching rate, for example, 600 Å/minute. The gate insulating film **104'** remains.

After removing the porous anodic oxide film **106**, an impurity element for giving the semiconductor layer one conductivity type is added by ion doping method with the gate electrode and the barrier type anodic oxide film **107** and the gate insulating film **104'** used as a mask in a self-aligning manner. As a result, high resistivity impurity regions **109** and **110** and low resistivity impurity regions (source and drain regions) **108** and **111** are formed. In the case of forming p-type regions, diborane (B_2H_6) is used as a dopant gas. The dose amount is 5×10^{14} to 5×10^{15} atoms/cm^2. The accelerating energy is 10-30 kV. After the introduction, the added impurity is activated by using a KrF excimer laser (wavelength 248 nm, pulse width 20 nsec).

When measuring the concentration of the impurity in the active layer by SIMS (secondary ion mass spectrometry), the impurity concentration in the source and drain regions **108** and **111** is 1×10^{20} to 2×10^{21} atoms/cm^3 and the impurity concentration in the high resistivity regions **109** and **110** is 1×10^{17} to 2×10^{18} atoms/cm^3. This corresponds to a dose of 5×10^{14}-5×10^{15} atoms/cm^2 in the former case and 2×10^{13} to 5×10^{14} atoms/cm^2 in the latter case. This difference is caused by the existence of the gate insulating film **104'**. Generally, the concentration is 0.5-3 times higher in the low resistivity impurity regions than in the high resistivity regions.

Then, an interlayer insulating film **114** of silicon oxide is formed on the entire structure by a CVD at 3000 Å thick, following which contact holes are formed through the insulating film and aluminum electrodes formed therein to contact the source and drain regions as shown in FIG. **1**F. Finally, a hydrogen annealing is performed to complete the formation of the TFT.

An example of an application of the TFT of the present inveution to a circuit substrate for an active matrix device such as a liquid crystal device will be explained with reference to FIG. **5**A. In FIG. **5**A, three TFTs are formed on a substrate. The TFT **1** and TFT **2** are used as driver TFTs in a peripheral circuit. The barrier type anodic oxide **501** and **502** in the TFT **1** and TFT **2** are 200-1000 Å thick, for example, 500 Å. Therefore, the gate electrode overlaps the high resistivity regions. The drain of TFT **1** and the source of TFT **2** are connected to each other, the source of TFT **1** is grounded, and the drain of TFT **2** is connected to a power source. Thus, a CMOS inverter is formed. It should not be limited to this configuration but any other circuits may be formed.

On the other hand, the TFT **3** is used as a pixel TFT for driving a pixel. The anodic oxide **503** is as thick as 2000 Å so that an offset area is formed. This configuration corresponds to the structure shown in FIG. **4**B. Accordingly, a leak curreut is reduced. One of the source and drain of the TFT **3** is connected to a pixel electrode **504** made of indium tin oxide (ITO). In the meantime, the TFTs **1** and **3** are N-channel type TFTs while the TFT **2** is a p-channel type TFT.

EXAMPLE 2

This example is an improvement of the Example 1, in which source and drain regions are provided with a silicide layer. Referring to FIG. **2**A, the reference numeral **201** shows a Corning 7059 glass substrate, **202**: a base film, **203**: a silicon island, **204**: an insulating film, **205**: an Al gate electrode (200 nm-1 μm thick), and **206**: a porous anodic oxide film (3000 Å-1 μm, e.g. 5000 Å thick). The same process as explained in the Example 1 is used to form these elements and the redundant explanation is omitted.

Referring to FIG. **2**B, a barrier type anodic oxide film **207** of 1000-2500 Å thick is formed in the same manner as in the Example 1 after the formation of the porous anodic oxide **206**. Then, a gate insulating film **204'** is formed by etching the insulating film **204** with the porous anodic oxide **206** used as a mask in a self-aligning manner.

Then, the porous anodic oxide **206** is removed by etching using the barrier type anodic oxide **207** as a mask. Further, ion doping of an impurity element (phosphorous) is carried out using the gate electrode **205** and the anodic oxide **207** as a mask in a self-aligning manner so that low resistivity

impurity regions **208** and **211** and high resistivity impurity regions **209** and **210** are formed as shown in FIG. **2**C. The dose amount is 1×10^{14}-5×10^{14} atoms/cm^2 and the acceleration voltage is 30-90 kV.

Referring to FIG. **2**D, a metal film **212** such as titanium is formed on the entire surface by sputtering. The thickness of the metal is 50-500 Å. The low resistivity regions **208** and **211** directly contacts the metal film. In place of titanium, other metals, for example, nickel, molybdenum, tungsten, platinum or paradium may be used.

Subsequently, a KrF excimer lascr (248 nm wavelength, 20 nsec pulse width) is irradiated onto the surface in order to activate the added impurity and form metal silicide regions **213** and **214** by reacting the metal film and the silicon in the active layer. The energy density of the laser beam is 200-400 mJ/cm^2, preferably, 250-300 mJ/cm^2. Also, it is desirable to maintain the substrate at 200-500° C. during the laser irradiation in order to avoid a peeling of the titanium film.

It is, of course, possible to use other light sources other than excimer laser. However, a pulsed laser beam is more preferable than a CW laser becausc an irradiation time is longer and there is a danger that the irradiated film is thermally expanded and peels off in the case of a CW laser.

As to examples of pulsed laser, there are a laser of an IR light such as Nd:YAG laser (Q switch pulse oscillation is preferred), a second harmonic wave of the Nd:YAG (visible light), and a laser of a UV light such as excimer laser of KrF, XeCl and ArF. When the laser beam is emitted from the upper side of the metal film, it is necessary to select wavelengths of the laser in order not to be reflected on the metal film. However, there is no problem when the metal film is enough thin. Also, it is possible to emit the laser from the substrate side. In this case, it is necessary to select a laser which can transmit through the silicon.

Also, instead of the laser annealing, a lump annealing of visible light or near infrared light may be employed. In such a case, the annealing is performed in order to heat the surface to 600-1000° C., for example, for several minutes at 600° C. or several tens seconds at 1000° C. An annealing with a near infrared ray (e.g. 1.2 μm) does not heat the glass substrate so much because the near infrared ray is selectively absorbed by silicon semiconductors. Further, by shortening the irradiation time, it is possible to prevent the glass from being heated.

Thereafter, referring to FIG. **2**E, only the titanium film remaining without converting into a silicide, for example, on the gate electrode or gate insulating film, is etched off by using an etchant containing hydrogen peroxide, ammonium and water at 5:2:2. As a result, titanium silicide **213** and **214** remain.

Referring to FIG. **2**F, an interlayer insulating film **217** is formed on the whole surface by depositing silicon oxide at 2000 Å-1 μm, for example, 3000 Å through CVD. Contact holes are formed through the insulating film **217** on the source and drain regions **213** and **214**, following which aluminum electrodes or wirings **218** and **219** having a thickness of 2000 Å-1 μm, e.g. 5000 Å are formed therein. The use of the metal silicide provides a stable interface with the aluminum as compared with the use of silicon semiconductors and provides a good contact with the aluminum electrode. The contact can be further improved by forming a barrier metal, for example, titanium nitride, between the aluminum electrodes **218** and **219** and the metal silicide regions **213** and **214**. The sheet resistance of the silicide regions can be made 10-50 Ω/square while that of the HRD **209** and **210** is 10-100 kΩ/square.

By the foregoing process, it is possible to improve the frequency characteristic of the TFT and suppress the hot carrier damage even with a higher drain voltage.

In this example, the low resistivity impurity region and the metal silicide region approximately coincide with each other. In particular, the edge **215** of the gate insulating film **204'** is approximately coextensive with the boundary **216** between the high resistivity impurity region **210** and the low resistivity impurity region **211** and also with the inner edge of the metal silicide region **214**. Thus, obviously, the explanations with reference to FIGS. **4**A-**4**D can be applied to this example by replacing the low resistivity region with the metal silicide region.

An application of this example to au active matrix device is shown in FIG. **5**B. In FIG. **5**B, three TFTs are formed on a substrate. The TFT **1** and TFT **2** are used as driver TFTs in a peripheral circuit. The barrier type anodic oxide **505** and **506** in the TFT **1** and TFT **2** are 200-1000 Å thick, for example, 500 Å. Therefore, the gate electrode overlaps the high resistivity regions. The drain of TFT **1** and the source of TFT **2** are connected to each other, the source of TFT **1** is grounded, and the drain of TFT **2** is connected to a power source. Thus, a CMOS inverter is formed. It should not be limited to this configuration but any other circuits may be formed.

On the other hand, the TFT **3** is used as a pixel TFT for driving a pixel. The anodic oxide **507** is as thick as 2000 Å so that an offset area is formed. This configuration corresponds to the structure shown in FIG. **4**B. Accordiugly, a leak current is reduced. One of the source and drain of the TFT **3** is connected to a pixel electrode **508** made of indium tin oxide (ITO).

In order to control the thickness of the anodic oxide of each TFT independently, the gate electrode of each TFT may preferably be made independent from one another. In the meantime, the TFTs **1** and **3** are N-channel type TFTs while the TFT **2** is a p-channel type TFT.

Also, the formation of the titanium film may be done before the ion doping of the impurity. In this case, it is advantageous that the titanium film prevents the surface from being charged up during the ion doping. Also, it is possible to carry out an annealing with laser or the like after the ion doping step but before the titanium forming step. After the titanium forming step, the titanium silicide can be formed by light irradiation or heat annealing.

EXAMPLE 3

This example is a further variation of Example **2**, in which the order of the formation of a metal silicide and the ion doping is changed. Referring to FIG. **3**A, on the Corning **7059** substrate **301** is formed a base oxide film **302**, island-like crystalline semiconductor (e.g. silicon) region **303**, silicon oxide film **304**, aluminum gate electrode **305** of 2000 Å to 1 μm, and a porous anodic oxide film **306** of 6000 Å on the side of the gate electrode. These are formed in the same manner as in the Example 1 as discussed with reference to FIGS. **1**A and **1**B.

Further, a barrier type anodic oxide film **307** is formed to 1000-2500 Å in the same manner as in the Example 1. Subsequently, the silicon oxide film **304** is patterned into a gate insulating film **304'** in a self-aligning manner as shown in FIG. **3**B.

Referring to FIG. **3**C, the porous anodic oxide **306** is removed in order to expose a part of the gate insulating film

304'. Subsequently, a metal layer such as titanium film **308** is formed on the entire surface by sputtering to a thickness of 50-500 Å.

Then, a KrF excimer laser is irradiated in order to form titanium silicide regions **309** and **310**. The energy density of the laser is 200-400 mJ/cm^2, preferably, 250-300 mJ/cm^2. Also, it is desirable to maintain the substrate at 200-500° C. in order to prevent the titanium film from peeling during the laser irradiation. This step may be carried out with lump annealing of a visible light or far infrared light.

Referring to FIG. **3**D, only the titanium film remaining, for example, on the gate electrode or gate insulating film, is etched off by using an etchant containing hydrogen peroxide, ammonium and water at 5:2:2. As a result, titanium silicide **309** and **310** remain.

Referring to FIG. **3**E, an ion doping of phosphorous is then performed using the gate electrode **305**, the anodic oxide **307** and the gate insulating film **304'** as a mask in order to form low resistivity impurity regions **311** and **314** and high resistivity impurity regions **312** and **313** at a dosc of 1-5×10^{14} atoms/cm^2 and an acceleration voltage 30-90 kV. The titanium silicide regions **309** and **310** approximately coincide with the low resistivity regions **311** and **314**, which in turn are source and drain regions.

Then, again, a KrF excimer laser (248 nm wavelength, 20 nsec pulse width) is irradiated in order to activate the added phosphorous. This may be carried out using a lump annealing of visible or far infrared ray as said above. Thereafter, the gate insulating film **304'** is etched with the gate electrode and the anodic oxide **307** used as a mask to form a gate insulating film **304"** as shown in FIG. **3**F. This is because the impurity added into the gate insulating film **304'** makes the device property instable.

In FIG. **3**F, an interlayer insulator **315** is formed on the entire surface by depositing silicon oxide at 6000 Å thick through CVD. Contact holes are opened through the insulator to form aluminum electrodes **316** and **317** on the source and drain regions. Thus, a TFT is completed.

In accordance with the present invention, the number of doping, or annealing steps can be reduced.

Moreover, an impurity such as carbon, oxygen or nitrogen may be added in addition to the p-type or n-type impurity ions in order to further reduce the reverse direction leak current and increase the dielectric strength. This is particularly advantageous when used for pixel TFTs in an active matrix circuit. In this case, the TFT **3** of FIGS. **5**A and **5**B has its anodic oxide film made the same thickness as the TFT **1** and TFT **2**.

EXAMPLE 4

A fourth example of the present invention will be explained with reference to FIGS. **7**A-**7**F. This example is comparative with the Example 1 and the same reference numerals show the same elements. Basically, each step is almost the same as the former examples so that redundant explanations will be omitted.

After forming a conductive film on the gate insulating film **104**, a mask material such as photoresist, photosensitive polyimide or a polyimide is formed on the entire surface of the conductive film. For example, a photoresist (OFPR 800/30 cp manufactured by Tokyo Oka) is spin coated. It is desirable to form an anodic oxide film between the conductive film and the photoresist. (not shown in the figure) Then, these films are patterned into the gate electrode **105** and a mask **117** as shown in FIG. **7**A. Then, in the same manner as in the Example 1, the porous anodic oxide film **106** is formed on the surface of the gate electrode **105** except for the portion on which the mask **117** is formed as shown in FIG. **7**B.

Then, referring to FIG. **7**C, the silicon oxide film **104** is patterned by dry etching in order to expose a part of the silicon film **103** to thus form the gate insulating film **104'**. The same etching method as is done in the Example 1 is also employed. Further, the photoresist mask is removed by conventional photolithography technique either before or after this etching step.

Referring to FIG. **7**D, the barrier type anodic oxide film **107** is formed in the same manner as in the Example 1 to a thickness of 2000 Å. Using this barrier type anodic oxide film as a mask, the porous anodic oxide is removed by phosphoric acid etchant as explained before. Accordingly, the structure shown in FIG. **7**E is obtained. The subsequent steps are identical to those explained with reference to FIGS. **1**E and **1**F.

Because the upper surface of the gate electrode is not oxidized in the first anodic oxidation, it is possible to prevent the thickness of the gate electrode from reducing too much during the first anodic oxidation. That is, in the Example 1, since the entire surface of the gate electrode is subjected to the anodic oxidation, the thickness of the gate electrode is reduced, causing the undesirable increase in the wiring resistance. This example avoids such a problem.

EXAMPLE 5

This example is a combination of the Example 2 and Example 4 and shown in FIGS. **8**A-**8**F. The steps shown in FIGS. **8**A-**8**B are exactly the same as the steps described with reference to FIGS. **7**A-**7**C of the Example 4. Namely, the porous anodic oxide is formed on only the side surface of the gate electrode while the upper portion of the gate electrode is covered with a mask. Also, the steps occurring after exposing the part of the silicon layer **203** as shown in FIG. **8**B, that is, the steps shown in FIGS. **8**C-**8**F, are identical to those explained in the Example 2 with reference to FIGS. **2**C-**2**F.

EXAMPLE 6

This example is also directed to a combination of the Example 3 and Example 5 and shown in FIGS. **9**A-**9**F. Namely, this example is different from the Example 5 only in the order of the formation of the metal silicide regions and the ion introducing step. Accordingly, the steps shown in FIGS. **9**A-**9**B are exactly the same as the steps described with reference to FIGS. **7**A-**7**C of the Example 4, which in turn corresponds to the steps shown in FIGS. **8**A and **8**B of the Example 5. The subsequent steps shown in FIGS. **9**C-**9**F exactly correspond to the steps shown in FIGS. **3**C-**3**F of the Example 3.

EXAMPLE 7

Referring to FIGS. **10**A-**10**F, this example is comparable with the Example 4 and shown in FIGS. **7**A-**7**F. The only difference is the order of the steps shown in FIGS. **10**C and **10**D. Namely, in FIG. **10**C, the barrier type anodic oxide film **107** is formed before etching the insulating film **104**. After the formation of the barrier type anodic oxide **107**, the insulating film **104** is patterned into the gate insulating film **104'**. On the other hand, in Example 4, the insulating film **104** is patterned before the barrier anodic oxide is formed as shown in FIG. **7**C. Accordingly, in the Example 7, the barrier

type anodic oxide protects the aluminum gate electrode **105** during the etching of the insulating film **104**.

EXAMPLE 8

This example is entirely the same as the Example 5 of FIGS. **8**A-**8**F except for the order between the step of patterning the gate insulating film and the step of forming the barrier type anodic oxide film **207**. Namely, referring to FIGS. **11**A-**11**B, the barrier type anodic oxide film **207** is formed before etching the part of the insulating film **204** as opposed to the Example 5. Thereafter, the insulating film is patterned into the gate insulating film **204'**. The subsequent steps shown in FIGS. **11**C-**11**F are entirely the same as those in the Example 5.

EXAMPLE 9

This example is also entirely the same as the Example 6 of FIGS. **9**A-**9**F except for the order between the step of patterning the gate insulating film **304** and the step of forming the barrier type anodic oxide film **307**. Namely, referring to FIGS. **12**A-**12**B, the barrier type anodic oxide film **307** is formed before etching the part of the insulating film **304**. Thereafter, the insulating film is patterned into the gate insulating film **304'**. The subsequent steps shown in FIGS. **12**C-**12**F are entirely the same as those in the Example 6.

Referring to Examples 6 to 9, although it has not been shown in the drawings, it is desirable to provide an anodic oxide film between the gate electrode and the mask when forming an anodic oxide film only on the side surface of the gate electrode. This feature will be described in more detail below with reference to FIGS. **13**A-**13**D.

FIGS. **13**A-**13**D show a fine wiring process using an anodizable material. On a substrate **701** which is for example, a silicon oxide film formed on a semiconductor, an aluminum film **702** is formed to a thickness of 2 μm, for example. Also, the aluminum may contain Sc (scandium) at 0.2 weight % to avoid an abnormal growth of the aluminum (hillock) during the subsequent anodizing step or may contain other additives such as yttrium (Y) to avoid an abnormal growth of the aluminum during a high temperature process.

Then, the aluminum film is anodic oxidized in an ethylene glycol solution containing 3% tartaric acid by applying a voltage of 10-30 V to the aluminum film. Thereby, a dense anodic oxide film **703** is formed on the aluminum film to a thickness of 200 Å. Then, using a photoresist mask **704**, the aluminum film **702** and the oxide film **703** are patterned in accordance with a predetermined pattern. Since the oxide film is enough thin so that it is easily etched at the same time.

In the case of the above patterning is carried out by isotropic etching, the edge of the patterned aluminum film has a shape as shown by numeral **707** in FIG. **13**B. Also, the difference in the etching rate between the oxide **703** and the aluminum **702** further enhances the configuration **17**.

Then, a porous anodic oxide film **705** is formed by applying a voltage of 10-30 V in an aqueous solution containing 10% oxalic acid. The oxidation mainly proceeds into the inside of the aluminum film.

It has been confirmed that the top end of the oxide growth, i.e. the boundary between the anodic oxide and the aluminum becomes approximately perpendicular to the substrate surface. On the other hand, in the case of the barrier type anodic oxide, the shape of the barrier type anodic oxide is almost conformal to the shape of the starting metal.

In this example, the thickness of the aluminum film is 2 μm and the porous anodic oxide film **705** grows at 5000 Å. The top end of the growth is approximately vertical when observing it through an electron microphotography.

After the formation of the porous anodic oxide film, the resist mask **704** is removed with a conventional releasing agent. Since the mask anodic oxide **703** is very thin, it may be peeled off at the same time with the resist mask **704**, or it may be removed in a later step by using a buffer hydrofluoric acid.

Further, as shown in FIG. **13**D, a barrier type anodic oxide film **706** of 2000 Å thickness is further formed by performing another anodic oxidation in a different condition. That is, the electrolyte is an ethylene glycol solution containing 3% tartaric acid and the applied voltage is about 150 V. This oxide film uniformly grows surrounding the aluminum film **702** from the boundary between the porous anodic oxide **705** and the aluminum film **702** in an inside direction.

Accordingly, a structure is formed in which a barrier type anodic oxide film is formed surrounding the aluminum film and further a porous type anodic oxide film is formed on the side of the aluminum film.

The porous anodic oxide **705** can be easily and selectively removed by a phosphoric acid, H_3PO_4 without damaging the aluminum.

Needless to say, the foregoing process can be employed to the anodic oxidation process of the foregoing Examples 4 to 9.

While a glass substrate is used in the foregoing examples, the TFT of the present invention may be formed on any insulating surface, for example, an organic resin or an insulating surface formed on a single crystalline silicon. Also, it may be formed in a three dimensional integrated circuit device. In particular, the present invention is particularly advantageous when used in an electro-optical device such as a monolithic type active matrix circuit which has a peripheral circuit formed on a same substrate.

Also, while crystalline silicon is used in the examples, the present invention is applicable to an amorphous silicon or other kinds of semiconductors.

While this invention has been described with reference to the preferred embodiments, it is to be understood that various modifications thereof will be apparent to those skilled in the art and it is intended to cover all such modifications which fall within the scope of the appended claims.

What is claimed is:

1. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a substrate, said semiconductor film including at least a first region to become a high resistance region and a second region to become a drain region adjacent to said high resistance region;

forming a gate insulating film over the semiconductor film;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film;

forming a metal film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said metal film contacts the second region of said semiconductor film so that a metal silicide layer is formed by a reaction between said metal film and the second region of said semiconductor film;

forming said high resistance region by adding an impurity to said first region for giving one conductivity type at a first concentration after forming the metal silicide layer; and

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the metal silicide layer,

wherein said metal silicide layer is not formed on the first region.

2. The method according to claim **1** wherein said metal film comprises a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

3. The method according to claim **1** wherein said impurity is an N-type impurity or a P-type impurity.

4. The method according to claim **1** wherein said metal silicide layer is formed after completing the formation of said metal film.

5. The method according to claim **1**, wherein the gate electrode comprises a metal layer.

6. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a substrate, said semiconductor film including at least a first region to become a high resistance region and a second region to become a drain region adjacent to said high resistance region;

forming a gate insulating film over the semiconductor film;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film;

forming a nickel film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said nickel film contacts the second region of said semiconductor film so that a nickel silicide layer is formed by a reaction between said nickel film and the second region of said semiconductor film;

forming said high resistance region by adding an impurity to said first region for giving one coductivity type at a first concentration after forming the nickel silicide layer; and

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the nickel silicide layer,

wherein said nickel silicide layer is not formed on the first region.

7. The method according to claim **6** wherein said impurity is an N-type impurity or a P-type impurity.

8. The method according to claim **6** wherein said nickel silicide layer is formed after completing the formation of said nickel film.

9. The method according to claim **6**, wherein the gate electrode comprises a metal layer.

10. A method for manufacturing a semiconductor device comprising the steps of:

forming a gate insulating film over a semiconductor film, said semiconductor film comprising silicon and including at least a first region to become a high resistance region and a second region to become a drain region adjacent to said high resistance region;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film;

forming a metal film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said metal film contacts the second region of said semiconductor film so that a metal silicide layer is formed by a reaction between said metal film and the second region of said semiconductor film;

forming said high resistance region by adding an impurity to said first region for giving one conductivity type at a first concentration after forming the metal silicide layer; and

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the metal silicide layer,

wherein said metal silicide layer is not formed on the first region.

11. The method according to claim **10** wherein said metal film comprises a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

12. The method according to claim **10** wherein said impurity is an N-type impurity or a P-type impurity.

13. The method according to claim **10** wherein said metal silicide layer is formed after completing the formation of said metal film.

14. The method according to claim **10**, wherein the gate electrode comprises a metal layer.

15. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a substrate, said semiconductor film including at least a first region to become a high resistance region and a second region to become a drain region adjacent to said high resistance region;

forming a gate insulating film over the semiconductor film;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film;

forming a metal film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said metal film contacts the second region of said semiconductor film;

formiug a metal silicide layer in said semiconductor film;

forming said high resistance region by adding an impurity to said first region for giving one conductivity type at a first concentration after forming the metal silicide layer; and

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the metal silicide layer.

16. The method according to claim **15**, wherein said metal film comprises a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

17. The method according to claim **15**, wherein said impurity is an N-type impurity or a P-type impurity.

18. The method according to claim **15**, wherein said metal silicide layer is formed after completing the formation of said metal film.

19. The method according to claim **15**, wherein the gate electrode comprises a metal layer.

20. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a substrate, said semiconductor film including at least a first region to become a high resistance region and a second region to become a drain region adjacent to said high resistance region;

forming a gate insulating film over the semiconductor film;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film:

forming a metal film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said metal film contacts the second region of said semiconductor film;

forming a metal silicide layer by irradiating said metal film and said semiconductor film with light;

forming said high resistance region by adding an impurity to said first region for giving one conductivity type at a first concentration after forming the metal silicide layer;

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the metal silicide layer.

21. The method according to claim **20** wherein said metal film comprises a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

22. The method according to claim **20** wherein said impurity is an N-type impurity or a P-type impurity.

23. The method according to claim **20** wherein said irradiation with light is conducted by using laser.

24. The method according to claim **20** wherein said irradiation with light is conducted by lamp annealing.

25. The method according to claim **20** wherein said nickel silicide layer is not formed on the first region.

26. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a substrate, said semiconductor film including at least a first region to become a high resistance region and a second region to become a drain region adjacent to said high resistance region;

forming a gate insulating film over the semiconductor film;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film;

forming a nickel film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said nickel film contacts the second region of said semiconductor film;

forming a nickel silicide layer by irradiating said nickel film and said semiconductor film with light;

forming said high resistance region by adding an impurity to said first region for giving one conductivity type at a first concentration after forming the metal silicide layer;

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the metal silicide layer.

27. The method according to claim **26** wherein said impurity is an N-type impurity or a P-type impurity.

28. The method according to claim **26** wherein said nickel silicide layer is not formed on the first region.

29. The method according to claim **26** wherein said irradiation with light is conducted by using laser.

30. The method according to claim **26** wherein said irradiation with light is conducted by lamp annealing.

31. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a substrate, said semiconductor film including at least a first region to become a high resistance region and a second region to become a drain region adjacent to said high resistance region;

forming a gate insulating film over the semiconductor film;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film;

forming a metal film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said metal film contacts the second region of said semiconductor film so that a metal silicide layer is formed by a reaction between said metal film and the second region of said semiconductor film;

forming said high resistance region by adding an impurity to said first region for giving one conductivity type at a first concentration after forming the metal silicide layer;

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the metal silicide layer; and

removing an unreacted portion of said metal film after the formation of said metal silicide layer by etching using a solution.

32. The method according to claim **31** wherein said metal silicide layer is not formed on the first region.

33. The method according to claim **31** wherein said metal film comprises a metal selected from the group consisting of titanium, nickel, molybdenum, tungsten, platinum and palladium.

34. The method according to claim **31** wherein said impurity is an N-type impurity or a P-type impurity.

35. The method according to claim **31** wherein said metal silicide layer is formed after completing the formation of said metal film.

36. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a substrate, said semiconductor film including at least a first region to become a high resistance region and a second region to became a drain region adjacent to said high resistance region;

forming a gate insulating film over the semiconductor film;

forming a gate electrode over the semiconductor film with the gate insulating film interposed therebetween wherein said second region of said semiconductor film is exposed from said gate insulating film;

forming a nickel film to cover said semiconductor film, said gate insulating film and said gate electrode wherein said nickel film contacts the second region of said semiconductor film so that a nickel silicide layer is

formed by a reaction between said nickel film and the second region of said semiconductor film;

forming said high resistance region by adding an impurity to said first region for giving one conductivity type at a first concentration after forming the metal silicide layer;

forming said drain region by adding an impurity to said second region for giving said one conductivity type at a second concentration higher than said first concentration after forming the metal silicide layer; and

removing an unreacted portion of said metal film after the formation of said metal silicide layer by etching using a solution.

37. The method according to claim **36** wherein said nickel silicide layer is not formed on the first region.

38. The method according to claim **36** wherein said impurity is an N-type impurity or a P-type impurity.

39. The method according to claim **36** wherein said nickel silicide layer is formed after completing the formation of said nickel film.

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(54) **SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME**

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Assistant Examiner—Stanetta D Isaac
(74) *Attorney, Agent, or Firm*—Nixon Peabody LLP; Jeffrey L. Costellia

(57) **ABSTRACT**

A low temperature process for fabricating a high-performance and reliable semiconductor device in high yield, comprising forming a silicon oxide film as a gate insulator by chemical vapor deposition using TEOS as a starting material under an oxygen, ozone, or a nitrogen oxide atmosphere on a semiconductor coating having provided on an insulator substrate; and irradiating a pulsed laser beam or an intense light thereto to remove clusters of such as carbon and hydrocarbon to thereby eliminate trap centers from the silicon oxide film.

Also claimed is a process comprising implanting nitrogen ions into a silicon oxide film and annealing the film thereafter using an infrared light, to thereby obtain a silicon oxynitride film as a gate insulator having a densified film structure, a high dielectric constant, and an improved-withstand voltage.

30 Claims, 7 Drawing Sheets

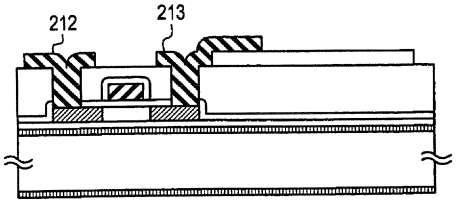

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FIG. 1A

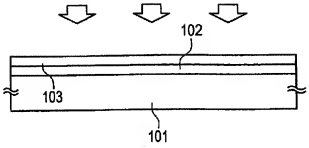
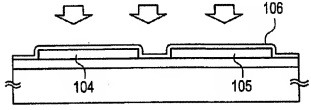


FIG. 1B



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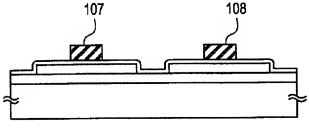


FIG. 1D

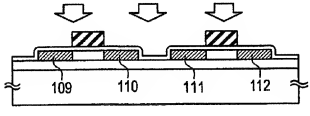


FIG. 1E

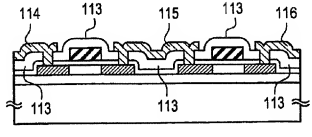


FIG. 2A

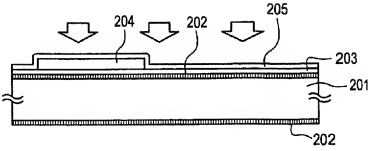
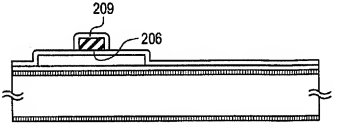


FIG. 2B



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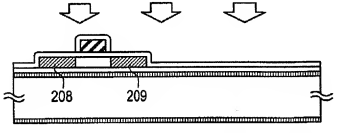


FIG. 2D

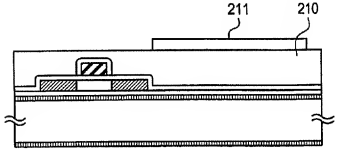
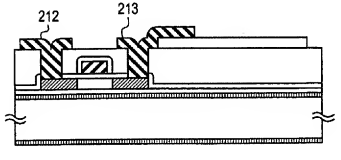


FIG. 2E



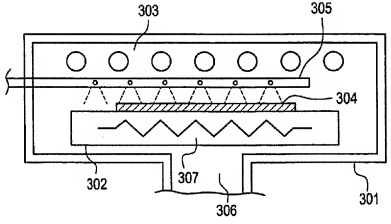


FIG. 3A

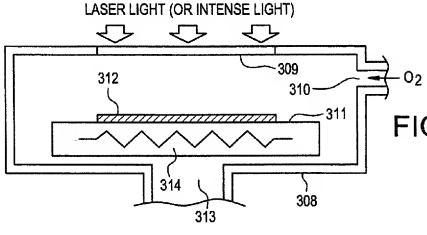


FIG. 3B

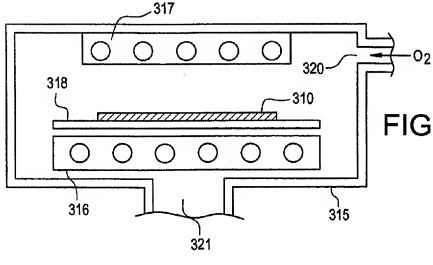


FIG. 3C

FIG. 4A

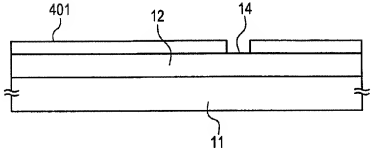


FIG. 4B

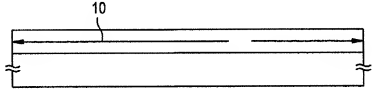


FIG. 4C

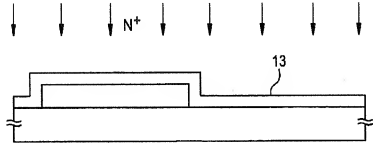


FIG. 4D

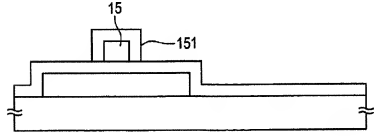


FIG. 5A

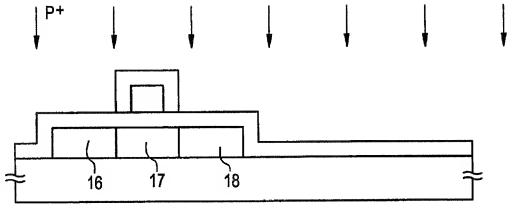


FIG. 5B

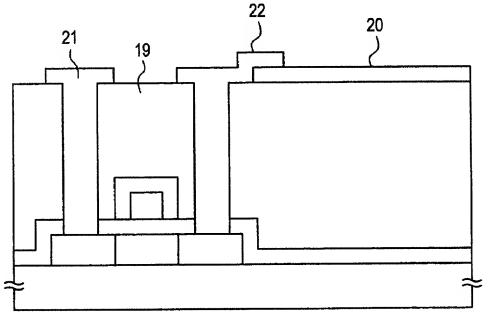


FIG. 6A

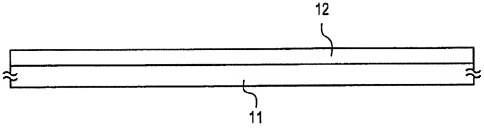


FIG. 6B

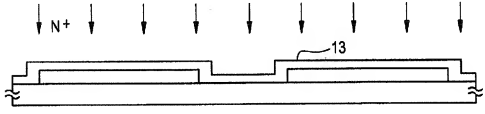


FIG. 6C

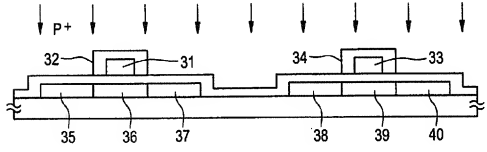


FIG. 6D

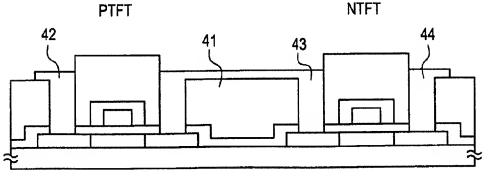


FIG. 7A

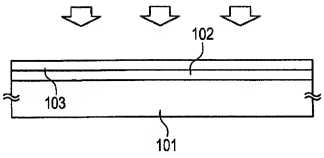


FIG. 7B

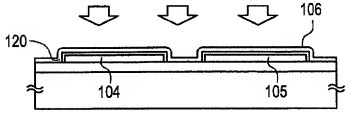


FIG. 7C

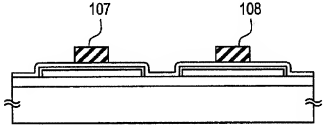


FIG. 7D

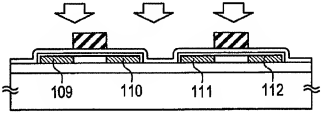
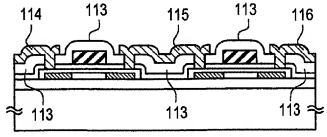


FIG. 7E



SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device using an insulator film, represented by a thin film transistor (referred to hereinafter as "TFT"), and to a process for fabricating the same. The present invention also relates to a process for fabricating, in high yield, a high-performance and reliable insulated gate semiconductor device on an insulator substrate under a temperature as low as 700° C. or even lower, and for fabricating an integrated circuit (IC) by assembling a plurality of such semiconductor devices.

The present device is useful as active matrices of liquid crystal displays, etc., driver circuits of image sensors, etc., and as TFTs of SOI (silicon on insulator) circuits and of conventional semiconductor ICs such as microprocessors, microcontrollers, microcomputers, and semiconductor memories.

2. Prior Art

Conventionally, liquid crystal display devices and image sensor devices are well known as devices using TFTs being integrated on a glass substrate. In general, insulated gate field effect semiconductor devices using thin film transistors are employed in the conventional devices above, and it is also customary to use a silicon oxide film as the gate insulators of those TFTs.

The TFTs using the silicon oxide film as the gate insulator, however, suffer problems such as the leak current ascribed to the pinholes in the gate insulator film, limits in increasing the film thickness (the capacity of a gate insulator depends on the film thickness and permittivity), instability in the required various properties as an insulator film due to the lack of density (that is, the film is too soft), and to the problems attributed to fixed charge such as sodium ions being incorporated in the gate insulator.

Recently, study is made intensively on the process for fabricating an insulated gate semiconductor device (MOSFET) on an insulator substrate. Those ICs having established on an insulator substrate are advantageous in their suitability to high speed drive, because, the ICs having established on an insulator need not suffer stray capacitance. In contrast to these ICs, the operation speed of a conventional IC is limited by a stray capacitance, i.e, a capacitance between the connection and the substrate. The MOSFETs having formed on an insulator substrate and having a thin film active layer is called a thin film transistor (TFT). A TFT can be found in a conventional semicoductor IC, for example, as a load transistor of an SRAM.

Furthermore, some of the recent products, for example, driver circuits for optical devices such as liquid crystal displays and image sensors, require a semiconductor IC to be formed on a transparent substrate. TFTs can be found assembled therein, but the ICs must be formed over a wide area and are thereby required that the TFTs are fabricated by a low temperature process. Furthermore, in devices having a plurality of terminals each connected with semiconductor ICs on an insulator substrate, for instance, it is proposed to reduce the mounting density by forming the first layer of the semiconductor IC or the entire semiconductor IC itself monolithically on the same insulator substrate.

Conventionally, the quality of TFTs have been ameliorated by providing a high performance (i.e., a sufficiently high mobility) semiconductor film by improving the crystallinity of an amorphous or a semi-amorphous film, or a microcrystalline film, by irradiating an intense light such as a laser beam thereto or by thermally annealing those films in the temperature range of from 450 to 1200° C. Amorphous TFTs using an amorphous material for the semiconductor film can be certainly fabricated; however, their application field is greatly limited by its inferior operation speed ascribed to too a low mobility of 5 cm^2/Vs or lower, about 1 cm^2/vs in general, or by its inability of providing a P-channel TFT (PTFT). A TFT having a mobility of 5 cm^2/vs or higher is available only after annealing the structure at a temperature in the range of from 450 to 1200° C. A PTFT can be fabricated only after subjecting the film to such annealing treatments.

However, in a process where a high temperature is required, in particular, only strictly selected substrate material can be used. More specifically, a so-called high temperature process which includes high temperature heating in the range of from 900 to 1,200° C. is advantageous, because it allows the use of a high quality film obtainable by thermal oxidation as a gate dielectric, but the usable substrates were confined to those made from expensive materials such as quartz, sapphire, and spinel, and they were not suited as substrates for large area applications.

In contrast to the high temperature process above, substrate materials can be selected from a wider variety in a low temperature process in which a maximum attainable temperature is 750° C. or lower for the entire process inclusive of a crystallization step using laser irradiating. However, there remains a problem of forming insulator films at a low temperature yet at a favorable step coverage and a high throughput. The insulator films can be deposited at a low temperature by sputtering, however, the process is still inferior considering its poor step coverage and insufficient throughput that results therefrom. Also known is depositing a silicon oxide film at a low temperature and high throughput by chemical vapor deposition (CVD) processes such as plasma CVD, low pressure CVD, and normal pressure CVD, in which a gasified organic material containing silicon atoms (referred to hereinafter as organic silane) such as tetraethoxysilane (TEOS) is used as the starting material. The resulting films, however, are rich in carbon atoms and hydrocarbon groups which develop into clusters to provide trap centers. Accordingly, those films are not suited for gate dielectrics because they fail to provide sufficiently high insulating properties and have too high interfacial level density.

The silicon oxide films using organic silane as the starting material as above cannot be used as-deposited for a material such as gate insulator film in which a sufficiently high electric properties are required. Accordingly, they were used only after subjecting them to an oxidation treatment at 700° C. or higher for a long duration of time. Such a heat treatment damages the substrate and impairs the throughput.

SUMMARY OF THE INVENTION

The present invention has been accomplished in light of the circumstances above.

Accordingly, an object of the present invention is to provide an oxide film at a low temperature and at excellent step coverage, yet with improved throughput and ameliorated film quality.

Another object of the present invention is to propose a process for fabricating a TFT, which can be performed at temperatures 700° C. or lower by combining various types of technology referred hereinbefore.

A further another object of the present invention is to overcome the problems above on the conventional gate insu-

lator films, and to thereby provide a TFT capable of yielding superior characteristics with high stability.

It has been now found that the objects above can be accomplished by the embodiments according to the present invention including the following.

A first embodiment of the present invention comprises forming a silicon oxide film by depositing a product obtained through decomposition of an organic silane (or a substituent product of organic silane comprising fluorine substituted for hydrogen, carbon or hydrocarbon radical thereof) by any of the CVD processes such as thermal CVD(chemical vapor deposition), plasma CVD(chemical vapor deposition), photo-CVD(chemical vapor deposition), and photo-plasma CVD (chemical vapor deposition), irradiating a light such as a laser pulse to the deposited film to modify the properties, particularly, by depriving the film of trap centers by removing carbon atoms and hydrocarbon groups from the film. In this manner, a silicon oxide film suitably used as a gate insulator film of a TFT can be obtained. The lasers for use in the present invention are pulsed lasers, and preferred are ultraviolet (UV) light emitting lasers such as excimer lasers, for example, the KrF^2, ArF, XeCl, and XeF lasers.

A second embodiment according to the present invention comprises forming a silicon oxide film by depositing a product obtained through decomposition of an organic silane by any of the CVD processes, exposing the resulting silicon oxide film to an oxidizing atmosphere comprising oxygen, ozone, nitrogen oxide, etc., and irradiating a UV light at a wavelength of 300 mm or shorter while heating the film to a temperature in the range of from 150 to 400° C., thereby removing the trap centers therefrom. In this manner, a silicon oxide film suitably used as a gate insulator film of a TFT can be obtained.

A further favorable effect can be obtained by combining the aforementioned first and second embodiments according to the present invention. For instance, a silicon oxide film obtained from an organic silane may be exposed to an oxidizing atmosphere and a UV light emitted from a laser at a wavelength of 300 nm may be irradiated thereto while heating the film to a temperature in the range of from 150 to 400° C.

Another embodiment according to the present invention comprises implanting nitrogen ions into a surface portion of an insulator film comprising a silicon oxide film having formed on the surface of a semiconductor to make a silicon oxinitride in the surface portion of the insulator film. The surface of the insulator film can be densified and the dielectric constant thereof be increased by thus surface nitriding the film. In particular, the present embodiment according to the present invention is characterized by implanting nitrogen ions into a surface portion of the silicon oxide film having deposited as the gate insulating film for the TFT (insulated gate field effect transistor), to thereby newly establish a silicon oxinitride film as the gate insulator. The silicon oxinitride film is expressed by SiO_xN_y, wherein x is from 0 to 2, preferably from 0.5 to 1.5, and y is from 0 to 4/3, preferably from 0.5 to 1.

The surface nitriding of the silicon oxide film is advantageous, because it densifies the film, increases the dielectric constant of the film to allow deposition of thicker films, and improves the general characteristics of the film as an insulator.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a step sequence diagram of a fabrication process for a TFT according to the present invention;

FIG. **2** shows a step sequence diagram of another fabrication process for a TFT according to the present invention;

FIG. **3** shows schematically drawn diagrams of laser and UV light treatment apparatuses for use in the present invention;

FIG. **4** shows a step sequence diagram of a fabrication process for a TFT according to a present example;

FIG. **5** shows a step sequence diagram of a fabrication process for another TFT according to another present example;

FIG. **6** shows a step sequence diagram of a fabrication process for another TFT according to another present example; and

FIG. **7** shows a step sequence diagram of another fabrication process for a TFT according to the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

A first embodiment of the present invention comprises forming a silicon oxide film by depositing a product obtained through decomposition of an organic silane by any of the CVD processes such as thermal CVD, plasma CVD, photo-CVD, and photo-plasma CVD, irradiating a pulsed laser beam to the deposited film to modify the properties, particularly, by depriving the film of trap centers by removing carbon atoms and hydrocarbon groups from the film. In this manner, a silicon oxide film suitably used as a gate insulator film of a TFT can be obtained. The lasers for use in the present invention are pulsed lasers, and preferred are UV light emitting lasers such as excimer lasers, for example, the KrF, ArF, XeCl, and XeF lasers.

An intense light preferably is UV or IR (infrared) light. UV light is, as described hereinafter, effective in driving carbon atoms and hydrocarbon groups out of the film. IR light rapidly heats the film to reduce the density of trap centers such as crystal defects and dangling bonds in the film.

The crystallinity of a semiconductor film may be modified, for example, from an amorphous state to a crystalline state by irradiating a laser beam or an IR light. As a matter of course, the crystallinity of the semiconductor film may be improved separately from the modification of the silicon oxide film.

A second embodiment according to the present invention comprises forming a silicon oxide film by depositing a product obtained through decomposition of an organic silane by any of the CVD processes, exposing the resulting silicon oxide film to an oxidizing atmosphere comprising oxygen, ozone, nitrogen oxide, etc., and irradiating a UV light at a wavelength of 300 mm or shorter while heating the film to a temperature in the range of from 150 to 400° C. to thereby remove the trap centers therefrom. In this manner, a silicon oxide film suitably used as a gate insulator film of a TFT can be obtained.

A further favorable effect can be obtained by combining the aforementioned first and second embodiments according to the present invention. For instance, a silicon oxide film obtained from an organic silane may be exposed to an oxidizing atmosphere and a UV light emitted from a laser at a wavelength of 300 nm may be irradiated while heating the film to a temperature in the range of from 150 to 400° C.

In general, organic silanes such as tetraethoxysilane (TEOS), inclusive of those containing fluorine as partial substituents for hydrocarbon groups, ethoxy groups, hydrogen atoms, etc., are liquid under an ordinary pressure and room temperature. Accordingly, they are heated under reduced pressure if necessary to introduce them into the reaction chamber in a gas phase. When a silicon oxide film is deposited

by plasma CVD, a pertinent amount of oxygen is mixed with organic silane and allowed to react using an inert gas such as argon and helium as a carrier gas. When the fabrication is to be performed by low pressure CVD or normal pressure CVD, a mixture of an organic silane and ozone is reacted, if necessary, using the carrier gases above.

In the processes above, the annealing for modifying the crystallinity of the semiconductor film is no longer a step determining the maximum temperature of the entire process, but other factors such as annealing for hydrogenation and annealing the gate oxide film become the determinative ones for the highest temperature of the process. This allows the substrate material to be selected from a wide variety of materials. More specifically, the maximum temperature of the process should he 700° C. or lower, and preferred maximum temperature is 400° C. or lower. As mentioned above, the process according to the present invention can he carried out at a temperature 700° C. or lower. Accordingly, the problems in the conventional processes, i.e., the pattern displacement in large area substrates due to thermal expansion, warping, etc., can be prevented from occurring in the process according to the present invention. For example, the process according to the present invention enables production of multiple TFTs at an extremely high precision from a large area substrate 300 mm×400 mm in size. It can be seen accordingly that the throughput can be increased by adopting the process of the present invention.

Furthermore, soda-lime glass, which had conventionally been regarded as a material unsuited for a substrate of a TFT due to its too low softening point, can be employed for operating thereon a TFT in the process according to the present invention after subjecting soda-lime glass to a proper treatment.

A method for forming a semiconductor device in accordance with the present invention comprises the steps of:

forming a semiconductor film on a substrate;

forming a protective insulating film on said semiconductor film, said protective insulating film being capable of transmitting a light;

irradiating a light to said semiconductor film to improve crystallinity of said semiconductor film;

removing said protective insulating film to expose a surface of said semiconductor film;

forming a silicon oxide film on the exposed surface by chemical vapor deposition using a raw material comprising organic silane;

irradiating a light to at least said silicon oxide film; and

forming a gate electrode on said silicon oxide film.

The light irradiated to the semiconductor film is a laser pulse or an infrared light. Also the irradiation of said light to said semiconduetor film is continued for 5 seconds to 5 minutes to elevate temperature of said semiconductor film up to 1000 to 1300° C. at a rate of 30 to 300° C./sec, and subsequently the temperature of said semiconductor film is descended at a rate of 30 to 300° C./sec. The light irradiated to at least the silicon oxide film is a laser pulse or an infrared light or a halogen light. Also the irradiation of said light to at least said silicon oxide film is continued for 5 seconds to 5 minutes to elevate temperature of said silicon oxide film up to 1000 to 1300° C. at a rate of 30 to 300° C./sec, and subsequently the temperature of said silieon oxide film is descended at a rate of 30 to 300° C./sec.

A first example of the application of the present invention comprises a peripheral circuit of an active matrix (AM) driven liquid crystal display device (LCD) using an amorphous silicon (a-Si) TFT. In general, an a-SiTFT-AMLCD can be fabricated by forming an a-SiTFT at a temperature 400° C. or lower on a alkali-free glass (such as Corning 7059) substrate. An a-SiTFT is best suited for a switching element from the viewpoint of its high OFF-resistance, however, as mentioned earlier, the operation speed is low and a CMOS cannot be fabricated therefrom. Accordingly, the peripheral circuits had been formed conventionally using single crystal ICs, and the terminals of the matrix had been connected to those of the ICs using a TAB (tape automated bonding) process and the like. Such a mounting process, however, becomes inapplicable with decreasing size of pixels, and, the cost therefor comes to account for a large part of the entire cost for fabricating the entire module.

It was not possible in the conventional process to form the peripheral circuit with the matrix on the same substrate. However, the inconvenience above can be circumvented in the process according to the present invention because a TFT having higher mobility can be formed at a temperature about the same as that necessary for forming an a-SiTFT.

According to a second example of the application of the present invention, a TFT can be formed on, for example, a soda-lime glass, i.e., a material less expensive than an alkali-free glass. In forming a TFT on a soda-lime glass substrate, it is preferred to form the TFT after first forming an insulator coating containing silicon nitride, aluminum oxide, etc., as the principal component on the surface of the glass substrate, and further forming an insulator basecoating film of a material such as silicon oxide and the like. In this manner, the mobile ions such as of sodium present in the glass can be prevented from intruding into the TFT. Additionally, the TFTs for the matrix can be formed with less failure by employing PTFTs rather than using NTFTs. The mobile ions which incidentally intrude into an NTFT from a substrate form a channel to turn the NTFT "ON", however, those which may intrude into a PTFT cannot form any channels.

A third example of the application of the present invention provides a peripheral circuit of a static drive simple matrix LCD. A ferroelectric liquid crystal (FLC) material has a memory effect, and hence, it can provide an image of high contrast ratio even when it is used in a simple matrix LCD. However, the peripheral circuit therefor had been established conventionally by connecting ICs by processes such as TAB in the same manner as that for an a-SiTFT-AMLCD. Similarly, TAB was used for connecting the peripheral circuits for the LCDs operating in a static manner based on the phase transition between a cholesteric phase and a nematic phase. A static drive LCD comprising a combination of a nematic liquid crystal and a ferroelectric polymer is also proposed in, for example, JP-A-61-1152 (the term "JP-A-" as referred herein signifies an "unexamined published Japanese patent application"), but the peripheral circuits are again connected by TAB.

Since the LCDs above are driven in a simple matrix, they can advantageously provide a large image plane using an inexpensive substrate yet with fine resolution. Images with high resolution can be obtained only by narrowing the pitch between the terminals, however, this can be realized at the expense of making the surface mounting of ICs difficult. The process according to the present invention enables the formation of peripheral circuits monolithically on an inexpensive substrate without taking the thermal problems into consideration.

A fourth example of applying the present invention includes a so-called three-dimensional IC which is fabricated by forming a TFT on a semiconductor IC furnished with metal connection.

Apparently, still various types of application are available from the present invention.

The present invention is illustrated in greater detail referring to non-limiting examples below. It should be understood, however, that the present invention is not to be construed as being limited thereto.

EXAMPLE 1

Referring to FIG. **1**, a method for forming a TFT (a semiconductor device) according to the present invention is described below. First, a silicon oxide film **102** was deposited as a base oxide film on a Corning 7059 substrate **101** (300 mm×300 mm in size; it may otherwise be 100 mm×100 mm in size) for a thickness of from 100 to 300 nm. The oxide film may be deposited by sputtering in an oxygen atmosphere or using plasma CVD which comprises decomposing TEOS and depositing the resulting product, followed by annealing the film in the temperature range of from 450 to 650° C.

An amorphous silicon film **103** was deposited thereafter by plasma CVD or by LPCVD for a thickness of from 30 to 150 nm, preferably for a thickness of from 50 to 100 nm. Then, a KrF excimer laser operating at a wavelength of 248 nm and a pulse, width of 20 nsec was irradiated to the film as shown in FIG. **1**(A) to improve the crystallinity of the silicon film **103**. The laser irradiation apparatus used herein is illustrated in FIG. **3**(B). The crystallinity of the film can be improved by a rapid thermal annealing (RTA) process which comprises irradiating a light as intense as the laser beam. It is also effective to further apply annealing using the above intense light to a silicon film having crystallized by irradiating a laser beam or by heating. An IR light such as a halogen light having a peak at a wavelength of 1.3 μm is particularly effective for selectively heating the silicon film, because a silicon film preferentially absorbs the light as compared with the glass substrate.

The laser irradiation was performed while heating the sample to a temperature in the range of from 150 to 400° C., and controlling the atmosphere to 10 mTorr or lower. As a result, a film of favorable crystallinity was obtained. The laser beam was irradiated at an energy density of from 200 to 400 mJ/cm^2, preferably from 250 to 300 mJ/cm^2. The crystallinity of the thus obtained silicon film **103** was studied by Raman scattering spectroscopy to observe a relatively broad peak at 515 cm^{-1} differing from a peak assigned to a single crystal silicon which should be found at 521 cm^{-1}.

The silicon layer **103** was patterned into island-like regions to give an NITFT region **104** and a PTFT region **105**. A gate oxide film **106** was formed thereon by decomposing TEOS and depositing a silicon oxide film from the decomposed product together with oxygen using RF plasma CVD (chemical vapor deposition) while controlling the temperature of the substrate in the range of from 200 to 500° C., preferably from 200 to 400° C., and more preferably, from 200 to 250° C. TEOS (as an organic silane) and oxygen were supplied at a pressure ratio of 1:1 to 1:3, while controlling the pressure in the range of from 0.05 to 0.5 Torr and the RF power in the range of from 100 to 250 W. This step may otherwise be conducted by low pressure CVD or normal pressure CVD using TEOS and ozone gas as the starting materials, while controlling the substrate temperature in the range of from 150 to 400° C., preferably from 200 to 250° C.

The resulting silicon oxide film was thermally annealed at 400 to 700° C. in an atmosphere comprising a nitrogen gas.

The as-deposited and annealed oxide film cannot be used as it is for a gate oxide film, because it contains a large amount of hydrocarbon groups which function as trap centers. In this context, a laser beam was irradiated to at least the silicon oxide film (the gate oxide film) using an apparatus illustrated in FIG. **3**(B) after the thermally annealing of the silicon oxide film to reduce the number of trap centers in the oxide film. Referring to FIG. **3**(B), the apparatus comprises a chamber **308** having provided with an oxygen gas inlet **310**, an exhaust port **313**, and a quartz window **309**, and a holder **311** equipped with a heater **314** is placed therein to mount thereon a sample **312**. A laser beam or an intense light is irradiated to the sample through the window **309**. The irradiation of an intense light reduces the trap centers in the oxide film in number, and, at the same time, densities the silicon oxide film and modifies the interface between the semiconductor and the silicon oxide film.

This step was performed as follows. First, the chamber was evacuated to a sufficiently high vacuum, and oxygen, ozone, or nitrogen oxide (e.g., NO_2, NO, and N_2O) was introduced therein to initiate the irradiation of a laser beam or an intense light. The irradiation was conducted under a reduced pressure of 10 Torr or lower, or under an oxidizing atmosphere of atmospheric pressure. Generally, a KrF laser beam is used as the laser beam. An intense light in general is an incoherent UV (ultraviolet light) light. When a laser is used, it should be operated for 10 shots at an energy density of from 250 to 300 mJ/cm^2. The temperature during the irradiation should be maintained preferably in the temperature range of from 150 to 400° C., and representatively, at 300° C. The application of RTO (rapid thermal oxidation) using an IR (infrared) light as the intense light, a halogen light at a wavelength of 1.3 μm, for instance, is also useful. The RTO process comprises instantaneous heating of the oxide film using an IR light to reduce the number of trap centers in the film. The irradiated surface is rapidly heated to a temperature in the range of from 1000 to 1300° C. preferably from 1,000 to 1,200° C. to modify the characteristics of the interface between the semiconductor and the gate oxide film. The interfacial level density of the gate oxide film can be reduced to 10^{11} cm^{-2} or lower by annealing. Also, in case of the RTO, a light may be irradiated to at least the gate oxide film for 5 seconds to 5 minutes to elevate temperature of the gate oxide film up to 1000 to 1300° C. at a rate of 30 to 300° C./sec followed by descending the temperature of the gate oxide film at a rate of 30 to 300° C./sec.

The resulting silicon oxide film was then thermally annealed at 400 to 700° C. in an atmosphere comprising a gas selected from the group consisting of nitrogen and oxygen.

An aluminum film was deposited at a thickness of from 200 nm to 5 μm using electron beam vapor deposition and was subjected to patterning to obtain gate electrodes **107** and **108** on the gate oxide film as shown in FIG. **1**(C). The aluminum film was deposited by electron beam deposition to obtain a film having high reflectance, because it should resist later to a laser irradiation. Thus was obtained an aluminum film so smooth that no grains were observed through an optical microscope. The grains as observed through an electron microscope was 200 nm or less in size. These grains must be controlled to a size smaller than the wavelength of the laser to be used in the process.

Impurities were implanted into the island-like silicon film of each of the TFTs by irradiating an ion to the island-like silicon film or by ion doping process in a self-aligned manner using the gate electrode as the mask. More specifically, phosphorus was first implanted at a dose of 2×10^{15} to 8×10^{15} cm^{-2} using phosphine (PH_3) gas as the doping gas, and after covering the island-like region **104** alone with a photoresist, boron was introduced at a dose of 4×10^{15} to 10×10^{15} cm^{-2} into solely the island-like region **105** using diborane (B_2H_6) as the doping gas. In this manner, boron was incorporated into the film at a dose higher than that of phosphorus.

Subsequently, a light such as a KrF laser beam 248 nm in wavelength was irradiated to the resulting structure at a pulse width of 20 nm with the gate electrode as a mask as illustrated in FIG. 1(D) to recover the crystallinity of the damaged impurity-doped regions. The apparatus used for this laser irradiation step is shown in FIG. 3(B). The laser was operated at an energy density in the range of from 200 to 400 mJ/cm^2, preferably in the range of from 250 to 300 mJ/cm^2. The sample iu this case was not beated. Thus were obtained N-type impurity (phosphorus) regions **109** and **110**, and P-type impurity (boron) regions **111** and **112**. The sheet resistance of these regions was found to be in the range of from 200 to 800 Ω/sq. A 300 nm thick silicon oxide film was deposited thereon as the interlayer insulator **113** using TEOS as the starting material in combination with oxygen in case of employing plasma CVD, or with ozone in case of carrying out low pressure CVD or normal pressure CVD. The temperature of the substrate was maintained throughout this step in the temperature range of from 150 to 400° C., preferably from 200 to 300° C.

Aluminum connections **114** to **116** were then formed after perforating contact holes in the source/drain of the TFTs. FIG. 1(E) shows an inverter circuit comprising an NTFT on the lcft hand side and a PTFT on the other side. The mobility for the TFTs was found to be from 50 to 100 cm^2/Vs for the NTFT and from 30 to 100 cm^2/Vs for the PTFT. Since the maximum process temperature in the present example is 400° C. or lower, no shrinking nor warping occurs on an alkali-free glass substrate such as Corning 7059 substrate. It follows that a large area display or a driver circuit therefor can be favorably fabricated from the above substrate, because substantially no displacement occurs on the patterns of the substrates as largc in size as above.

EXAMPLE 2

Rcferring to FIG. **2**, a process for fabricating a TFT on a soda-limc glass substrate to provide an AMLCD elemcut according to the present invention is described below. First, a silicon nitride film **202** was depositedas a blocking layer over the entire surface of a substrate **201** made from a soda-lime glass plate 1.1 mm in thickness and 300 mmx400 mm in size. Bccause a soda-limc glass is abundant in sodium, the silicon nitride film **202** as the blocking layer was deposited by plasma CVD process at a thickness of from 5 to 50 nm, prcferably from 5 to 20 nm, to thereby prevent sodium diffusion from occurring in the TFT. This technology of providing a blocking layer by coating the substrate with a silicon nitride or aluminum oxide film is disclosed in Japanese patent application Nos. Hei-3-238710 and Hei-3-238714 filed by the prcsent applicants.

Subsequent to the formation of a base oxide (silicon oxide) layer **203**, a silicon film **204** was deposited at a thickness of from 30 to 150 nm, preferably from 30 to 50 nm by LPCVD or plasma CVD. The film was subjected to debydrogenation at 400° C. for a duration of one hour and then patterned to form island-likc semiconductor regions as the active layer of the TFT. A gate insulator film **205** was deposited for a thickness of from 70 to 120 nm, typically for a thickness of 100 nm, in an oxygen atmosphere by plasma CVD using TEOS as the starting material. The substrate was maintained at a temperature of 400° C. or lower, preferably in the range of from 200 to 350° C., to prevent shrinking or warping from occurring on the substrate. The resulting silicon oxide film, however, contains numerous hydrocarbon groups and many trap centers. More specifically, for example, the interfacial level density was found to be 10^{12} cm^{-2} or more, a value far beyond the allowable density for a gate insulator film.

Accordingly, a laser beam emitted from a KrF laser or a light having an intensity equivalent thereto was irradiated to the gate insulator film **205** and the island-like semiconductor regions **204** as shown in FIG. 2(A) to improve the crystallinity of the island-like semiconductor regions and to ameliorate the characteristics of the gate insulator film **205** by reducing the number of the trap centers therein. That is, the present step encompasses both the crystallization of the silicon film and the modification of the gate oxide film, which were conducted separately in two steps in the foregoing Example 1. If an intense light were to be employed, annealing using an IR light, a halogen light 1.3 μm in wavelength, for instance, is particularly effective in this case.

The laser irradiation in this step is preferably performed in the presence of oxygen in excess, under a reduced pressure of 10 Torr or lowcr. A reduced pressure is preferred because the carbon atoms present in the oxide film may readily be desorbed. The oxygen partial pressure was controlled, for example, in the range of from 1 to 10 Torr. The laser beam was irradiated at an energy density of from 250 to 300 mJ/cm^2, and was shot for 10 times. Preferably, the temperature is maintained in the range of from 150 to 400° C., and representatively, at 300° C. The laser irradiation was conducted using an apparatus illustrated in FIG. 3(B). A silicon film **204** improved in crystallinity and a gate oxide film reduced in interfacial level density to 10^{11} cm^{-1} or lower were obtained as a result.

After forming an aluminum gate electrodc **208** in the same manner as in Example 1, the entire structure together with the substrate was immcrsed into an electrolytic solution as an anode, and current was applied thereto to form an anodic oxide coating **209** for a thickness of 206 nm on the surface of the aluminum connection inclusive of the gate electrode. The technique of anodic oxidation is disclosed in Japanese patent application Nos. Hei-4-30220, Hei-4-38637, and Hei-4-54322 filed by the present applicants. The structure obtained after this step is shown in FIG. 2(B). Otherwise, a negative voltage can be reversely applied to the structure upon completion of the anodic oxidation; for example, a voltage in the range of from −100 to −200 V may be applied for a duration of from 0.1 to 5 hours, while maintaining the substrate preferably in the range of from 100 to 250° C., representatively at 150° C. By incorporating this additional step, the mobile ions inside silicon oxide or at the boundary between silicon oxide and silicon are attracted to the aluminum gate clectrodc. This technique of applying a negative voltage to the gate electrode after or during anodic oxidation is disclosed in Japanese patent application No. Hei-4-1155-3 filed by the present applicants on Apr. 7, 1992.

Boron as a P-type impurity was then implanted into the silicon layer in a self-aligned manner by ion doping to form source/drain **208** and **209** of the TFT, and a KrF laser beam having set at an energy density of from 250 to 300 mJ/cm^2 was irradiated thereto to recover the crystallinity of the silicon film having damaged by the ion doping process. The sheet resistance of the source/drain after the laser irradiation was found to be in the range of from 300 to 800 Ω/sq. Annealing by irradiating an intense light, preferably an IR light, is useful in this step.

A pixel contact **211** was formed using an ITO after forming an interlayer insulator **210** using polyimide. Contact holes were perforated thereafter to establish contacts **212** and **213** in the source/drain regions of the TFTs using a chromium/aluminum multilayered film composed of a 20 to 200 nm thick, representatively 100 nm thick, lower chromium film

and a 100 to 2,000 nm thick, representatively 500 nm thick, upper aluminum film. The multilayers are preferably deposited continuously using sputtering. One **213** of the thus obtained two contacts was connected to the ITO. Finally, the structure was annealed in hydrogen at 200 to 300° C. for a duration of 2 hours to complete the hydrogenation of silicon. Thus was obtained a complete TFT. A plurality of such TFTs having fabricated simultaneously were assembled in a matrix to obtain an AMLCD device.

EXAMPLE 3

Referring to FIG. **1**, a process for fabricating another TFT according to the present inventiou is described below. First, a silicon oxide film **102** was deposited as a base oxide film on a Corning 7059 substrate **101** for a thickness of from 100 to 300 nm. An amorphous silicon film **103** was deposited thereafter by plasma CVD or by LPCVD for a thickness of from 30 to 150 nm, preferably for a thickness of from 50 to 100 nm. Then, a KrF^2 excimer laser operating at a wavelength of 248 nm and a pulse width of 20 nsec was irradiated to the film as shown in FIG. **1**(A) to improve the crystallinity of the silicon film **103**. The crystallinity of the film can be improved by irradiating a light as intense as the laser beam to heat the silicon film to a temperature range of from 1,000 to 1,200° C.

The silicon layer **103** was patterned into island-like regions to give an NTFT region **104** and a PTFT region **105**. A gate oxide film **106** was formed thereon by decomposing TEOS (organic silane) and depositing a silicon oxide film from the decomposed product together with oxygen using RF plasma CVD. The as-deposited oxide film cannot be used as it is for a gate oxide film, because it contains a large amount of hydrocarbon groups which function as trap centers. In this context, a laser beam was irradiated together with an intense light using an apparatus illustrated in FIG. **3**(A) to reduce the number of trap centers in the oxide film. This step also densifies the oxide film. The intense light may be a UV (ultraviolet) light or an IR light which accompanies rapid heating. Referring to FIG. **3**(A), the apparatus comprises a chamber **301** having provided with an oxygen gas inlet **305** which provides an oxygen gas shower, an exhaust port **306**, and a UV lamp **303**; a holder **302** equipped with a heater **307** is placed therein to mount a sample **304** thereon. A UV (ultraviolet) light having a wavelength of 300 nm or shorter is irradiated to at least the gate oxide film to effect the annealing. A 40-W UV lamp which emits a light having a spectrum with a peak at a wavelength of approximately 250 nm was used in this apparatus.

In the chamber, a shower of oxygen, ozone, or nitrogen oxide (e.g., NO_2, NO, and N_2O) was blown against the sample. No particular step of evacuating the chamber to vacuum was carried out. Accordingly, UV light irradiation was effected under atmospheric pressure. The UV light causes the oxidizing gas to undergo a photochemical reaction to generate active oxygen or ozone. These active species then react with carbon, hydrocarbons, etc., inside the silicon oxide film to decrease the concentration of the carbon atoms inside the film to a sufficiently low level. Preferably, the sample is maintained iu a temperature range of from 150 to 400° C., representatively at 300° C. during the reaction. As a result, the interfacial level density was reduced to 10 cm^{-2} or lower.

An apparatus shown in FIG. **3**(C) can be used in the place of the one shown in FIG. **3**(A). Referring to FIG. **3**(C), the apparatus comprises a chamber **315** having provided with an oxygen gas inlet **320**, an exhaust port **321**, and a UV lamp **317**; a holder **318** is placed therein to mount a sample **319** thereon. In this apparatus, an oxidizing gas such as oxygen, ozone, and a nitrogen oxide is introduced after evacuating the chamber to a sufficiently high vacuum.

An aluminum film was deposited at a thickness of from 200 nm to 5 μm using electron beam vapor deposition and was subjected to patterning to obtain gate electrodes **107** and **108** on the gate oxide film as shown in FIG. **1**(C). Impurities were implanted into the island-like silicon film of each of the TFTs by ion doping process in a self-aligned manner using the gate electrodes as the masks. A KrF^2 laser beam 248 nm in wavelength was irradiated to the resulting structure at a pulse width of 20 nm as illustrated in FIG. **1**(D) to recover the crystallinity of the damaged impurity-doped regions. Thus were obtained N-type impurity (phosphorus) regions **109** and **110**, and P-type impurity (boron) regions **111** and **112**. The sheet resistance of these regions was found to be in the range of from 200 to 800 Ω/sq. A 300 nm thick silicon oxide film was deposited thereon as the interlayer insulator **113** using TEOS as the starting material.

Aluminum connections **114** to **116** were then formed after perforating contact holes in the source/drain of the TFTs. FIG. **1**(E) shows an inverter circuit comprising an NTFT on the left hand side and a PTFT on the other side. The mobility for the TFTs was found to be from 50 to 100 cm^2/Vs for the NTFT and from 30 to 100 cm^2/Vs for the PTFT. Thus was obtained a five-digit shift resister, and its driving at 10 MHz or higher was confirmed at a drain voltage of 20 V.

EXAMPLE 4

Referring to FIG. **7**, a process for fabricatiug a TFT according to the preseut invention is described below. First, a silicon oxide film **102** was deposited as a base oxide film on a Corning 7059 substrate **101** (300 mm×300 mm in size, which may otherwise be 100 mm×100 mm in size) for a thickness of from 100 to 300 nm. The oxide film may be deposited by sputtering in an oxygen atmosphere or using plasma CVD which comprises decomposing TEOS and depositing the resulting product, followed by annealing the film in the temperature range of from 450 to 650° C.

An amorphous silicon film **103** was deposited thereafter by plasma CVD or by LPCVD for a thickness of from 30 to 150 nm, preferably for a thickness of from 50 to 100 nm. Then, a KrF^2 excimer laser operating at a wavelength of 248 nm and a pulse width of 20 nsec was irradiated to the film as shown in FIG. **7**(A) to improve the crystallinity of the silicon film **103**. The laser irradiation apparatus used herein is illustrated in FIG. **3**(B). The crystallinity of the film can be improved by a rapid thermal annealing (RTA) process which comprises irradiating a light as intense as the laser beam. It is also effective to further apply annealing using the above intense light to a silicon film having crystallized by irradiating a laser beam or by heating. An IR light such as a halogen light having a peak at a wavelength of 1.3 μm is particularly effective for selectively heating the silicon film, because, as compared with the glass substrate, a silicon film prefereutially absorbs the light.

The laser irradiation was performed while heating the sample to a temperature in the range of from 150 to 400° C., and controlling the atmosphere to 10 mTorr or lower. As a result, a film of favorable crystallinity was obtained. The laser beam was irradiated at an energy density of from 200 to 400 mJ/cm^2, preferably from 250 to 300 mJ/cm^2. The crystallinity of the thus obtained silicon film **103** was studied by Raman scattering spectroscopy to observe a relatively broad peak at 515 cm^{-1} differing from a peak assigned to a single crystal silicon which should be found at 521 cm^{-1}.

The silicon layer **103** was patterned into island-like regions to give an NTFT region **104** and a PTFT region **105**. The

surface portion of the island-like NTFT and PTFT regions **104** and **105** was oxidized at a temperature range of from 500 to 700° C. in an oxide gas to form a 20 to 200 Å thick first silicon oxide layer **120**. The oxide gas may be, for example, a 99.9% or higher purity dry oxygen. A gate oxide film **106** was formed on the first silicon oxide layer as a second silicon oxide layer by decomposing TEOS (organic silane) and depositing a silicon oxide film from the decomposed product together with oxygen using RF plasma CVD (chemical vapor deposition) while controlling the temperature of the substrate in the range of, from 200 to 500° C., preferably from 200 to 400° C., and more preferably, from 200 to 250° C. TEOS and oxygen were supplied at a pressure ratio of 1:1 to 1:3, while controlling the pressure in the range of from 0.05 to 0.5 Torr and the RF power in the range of from 100 to 250 W. This step may otherwise be conducted by low pressure CVD or normal pressure CVD using TEOS and ozone gas as the starting materials, while controlling the substrate temperature in the range of from 150 to 400° C., preferably from 200 to 250° C.

The resulting silicon oxide film was thermally annealed at 400 to 700° C. in a nitrogen gas atmosphere.

The as-deposited and annealed oxide film cannot be used as it is for a gate oxide film, because it contains a large amount of hydrocarbon groups which function as trap centers. In this context, a laser beam was irradiated to at least the first and second silicon oxide layers using an apparatus illustrated in FIG. 3(B) to reduce the number of trap centers in the oxide film. A light may he irradiated to at least the first and second silicon oxide layers for 5 seconds to 5 minutes to elevate temperature of said first and second oxide layers up to 1000 to 1300° C. at a rate of 30 top 300° C./sec. followed by descending the temperature of said first and second silicon oxide layers at a rate of 30 to 300° C./sec. Referring to FIG. 3(B), the apparatus comprises a chamber **308** having provided with an oxygen gas inlet **310**, an exhaust port **313**, and a quartz window **309**; a holder **311** equipped with a heater **314** is placed therein to mount thereon a sample **312**. A laser beam or an intense light is irradiated to the sample through the window **309**. The irradiation of an intense light reduces the number of the trap centers in the oxide film, and, at the same time, densities the silicon oxide film and modifies the interface between the semiconductor and the silicon oxide film.

This step was performed as follows. First, the chamber was evacuated to a sufficiently high vacuum, and oxygen, ozone, or nitrogen oxide (e.g., NO_2, NO, and N_2O) was introduced therein to initiate the irradiation of a laser beam or an intense light. The irradiation was conducted under a reduced pressure of 10 Torr or lower, or under an oxidizing atmosphere of atmospheric pressure. Generally, a KrF^2 laser beam is used as the laser beam. An intense light in general is an incoherent UV light. When a laser is used, it should be operated for 10 shots at an energy density of from 250 to 300 mJ/cm^2. The temperature during the irradiation should be maintained preferably in the temperature range of from 150 to 400° C., and representatively, at 300° C. The application of RTO (rapid thermal oxidation) using an IR light as the intense light, a halogen light at a wavelength of 1.3 μm, for instance, is also useful. The RTO process comprises instantaneous heating of the oxide film using an IR light to reduce the number of trap centers in the film. The irradiated surface is rapidly heated to a temperature in the range of from 1,000 to 1,200° C. to modify the characteristics of the interface between the semiconductor and the gate oxide film. The interfacial level density of the gate oxide film can be reduced to 10^{11} cm^{-2} or lower by annealing.

The resulting silicon oxide film was then thermally annealed at 400 to 700° C. in a nitrogen or oxygen gas atmosphere.

An aluminum film was deposited at a thickness of from 200 nm to 5 μm using electron beam vapor deposition and was subjected to patterning to obtain gate electrodes **107** and **108** as shown in FIG. 7(C). The aluminum film was deposited by electron beam deposition to obtain a film having high reflectance, because it should resist later to laser irradiation. Thus was obtained an aluminum film so smooth that no grains were observed through an optical microscope. The grains as observed through an electron microscope was 200 nm or less in size. These grains must be controlled to a size smaller than the wavelength of the laser to be used in the process.

Impurities were implanted into the island-like silicon film of each of the TFTs by ion doping process in a self-aligned manner using the gate electrodes as the masks. More specifically, phosphorus was first implanted at a dose of 2×10^{15} to 8×10^{15} cm^{-2} using phosphine (PH_3) gas as the doping gas, and after covering the island-like region **104** alone with a photoresist, boron was introduced at a dose of 4×10^{15} to 10×10^{15} cm^{-2} into solely the island-like region **105** using diborane (B_2H_6) as the doping gas. In this manner, boron was incorporated into the film at a dose higher than that of phosphorus.

A KrF laser beam 248 nm in wavelength was irradiated to the resulting structure at a pulse width of 20 nm as illustrated in FIG. 7(D) to recover the crystallinity of the damaged impurity-doped regions. The apparatus used for this laser irradiation step is shown in FIG. **3**(B). The laser was operated at an energy density in the range of from 200 to 400 mJ/cm^2, preferably in the range of from 250 to 300 mJ/cm. The sample in this case was not heated. Thus were obtained N-type impurity (phosphorus) regions **109** and **110**, and P-type impurity (boron) regions **111** and **112**. The sheet resistance of these regions was found to be in the range of from 200 to 800 Ω/sq. A 300 nm thick silicon oxide film was deposited thereon as the interlayer insulator **113** using TEOS as the starting material in combination with oxygen in case of employing plasma CVD, or with ozone in case of carrying out low pressure CVD or normal pressure CVD. The temperature of the substrate was maintained throughout this step in the temperature range of from 150 to 400° C., preferably from 200 to 300° C.

Aluminum connections **114** to **116** were then formed after perforating contact holes in the source/drain of the TFTS. FIG. 7(E) shows an inverter circuit comprising an NTFT on the left hand side and a PTFT on the other side. The mobility for the TFTs was found to be from 50 to 100 cm^2/Vs for the NTFT and from 30 to 100 cm^2/Vs for the PTFT. Since the maximum process temperature in the present example is 400° C. or lower, no shrinking nor warping occurs on an alkali-free glass substrate such as Corning 7059 substrate. It follows that a large area display or a driver circuit therefor can be favorably fabricated from the above substrate, because substantially no displacement occurs on the patterns of the substrates as large in size as the one described above.

EXAMPLE 5

An example of forming an NTFT (insulated gate field effect transistor) on the pixel electrode portion of an AMLCD device is described below. As a matter of course, the basic structure is the same for various types of modifications such as a PTFT having formed in the place of the NTFT and the TFTs having formed for the peripheral circuit of a liquid crystal display device. Furthermore, a structure similar to that in the present example can be used as the basic structure of the TFTs for image sensors and other types of ICs.

Referring to FIGS. **4** and **5**, the fabrication process for the present example is described. Referring to FIG. **4**, a 2,000 Å thick silicon oxide film (not shown in the figure) was deposited by sputtering on a glass substrate **11** as a base coating. According to a known technology, a 1,000 Å thick amorphous silicon film **12** was deposited thereon by plasma CVD. A mask **401** provided with a portion **14** to expose the underlying amorphous silicon film, was then formed using silicon oxide at a thickness of 500 Å.

Subsequently, a 20 Å thick nickel silicide film was deposited by sputtering. This film is incorporated to accelerate the crystallization of the underlying amorphous silicon film **12** with the constituent element nickel. This film in general is deposited to a thickness of from 5 to 200 Å. Nickel was used in this case for accelerating the crystallization of the amorphous silicon film, but any element belonging to Group VIII of the periodic table, such as iron (Fe), cobalt (Co), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), and platinum (Pt), may be used in the place of nickel. Also usable are those belonging to Group IIId of the periodic table, and specifically mentioned are scandium (Sc), titanium (Ti), vanadium (V), chromium (Cr), manganese (Mn), copper (Cu), and zinc (Zn). Gold (Au) and silver (Ag) are also members useful in the present invention. Particularly preferred among them are Ni, Pd, Cu, and Au. These elements may be incorporated in the film by any means, such as depositing a thin film on the upper or the lower surface of the amorphous silicon film by using sputtering, plasma treatment which comprises sputtering using a plasma, CVD, and vapor deposition, and directly introducing the elements into the amorphous silicon film by using ion implantation.

The silicon oxide film **401** mask was removed thereafter to leave nickel silicide film selectively on the surface portion **14** of the amorphous silicon film **12**. Then, nickel in the surface portion **14** of the amorphous silicon film was alloydized by irradiating an IR light, for example, at a wavelength of 1.3 μm, to instantaneously heat the selected surface portion of the amorphous silicon film. In this manner, a nickel silicide portion can be formed. This step is useful for effective crystallization, because it facilitates nickel diffusion in the later step of annealing for the crystallization.

An annealing for 4 hours at 550° C. in an inert gas atmosphere was effected thereafter. The heat treatment allows the amorphous silicon film **12** to crystallize. During this step, the crystallization occurs along a direction parallel to the substrate as indicated with arrows **10** in the figure to give acicular or columnar crystals. The crystal growth occurs over a distance of 40 μm or longer. The crystallization process need not always follow the one described above, and a laser beam may be irradiated or a thermal annealing at 600° C. for a duration of 24 hours or longer may be performed according to known techniques. Furthermore, the film may be left amorphous (see FIG. **4**(B) for reference).

Then, an active layer is established by isolating the elements. The active layer herein refers to the region in which source/drain regions and channel forming regions are to be formed. Preferably the nickel-containing region **14** into which nickel was introduced in the form of nickel silicide and the final point of the crystal growth (i.e., the left end of the silicon film **12** in the figure) are removed by etching, because these portions contain nickel in an excessively high concentration. The remaining intermediate portion having grown parallel to the substrate can be favorably used as the active layer.

Subsequent to the step above, a 1,500 Å thick silicon oxide film **13** was formed for a gate insulator film. The incorporation of chlorine atoms into this silicon oxide film is preferred, because the film then exerts gettering effect on impurity ions.

Referring to FIG. **4**(C), nitrogen ions are implanted into the silicon oxide film **13**. A silicon oxynitride surface forms on the surface of the silicon oxide film in this step. However, intrusion of nitrogen ions into the active layer through the silicon oxide film **13** must be avoided. The key in this step is to nitride only the vicinity of the surface of the silicon oxide film **13**.

A silicon oxynitride film **13** having a dielectric constant of from 4 to 6 results by the implantation of the nitrogen ions in the step above. The dielectric constant of from 4 to 6 is higher as compared to that of 3.8 to 4.0 of the silicon oxide film. Moreover, the film itself can be densified. As a result, problems such as of impurity ion (sodium ion) transport within the gate insulator film, leakage ascribed to pinholes, and withstand voltage can be solved. Furthermore, a thicker gate insulator film can be established because the dielectric constant therefor is higher than that for the silicon oxide film. This advantage favors solving the problems of leak current and pinholes.

Also preferred is to apply photo-annealing by irradiating an infrared ray to the silicon oxide gate insulator film **13** after implanting nitrogen ions into the silicon oxide gate insulator film **13**. Particularly preferred is the use of a near IR light about 1 to 2 μm in wavelength, because the defects and the dangling bonds in the silicon film **12** can be eliminated without heating the glass substrate, and because the interfacial level density between the gate insulator film **13** and the silicon film **12** can be lowered at the same time. These greatly contribute to the improvement of the TFT characteristics.

A gate contact **15** was formed by patterning a 6,000 Å thick aluminum film having formed on the gate insulator film **13**. The surface of the gate contact **15** was oxidized by anodic oxidation to form an oxide layer **151** on the surface of the gate contact **15**. This oxide layer **151** is used in the later step of ion implantation to form an offset gate structure, and the thickness thereof determines the offset gate length. Accordingly, the oxide layer was formed at a thickness of 2,000 Å in this example. The resulting structure is shown in FIG. **4**(D).

The gate contact in the present example can be formed using a known material based on silicon.

Referring to FIG. **5**(A), source/drain regions **16** and **18**, and a channel forming region **17** were formed in a self-aligned manner after introducing phosphorus (P) by ion implantation. Subsequently, laser beam or IR light was irradiated to anneal the source/drain regions.

A polyimide film was formed as an interlayer insulator **19**, and an ITO electrode **20** as a pixel electrode was formed thereon. Source/drain electrodes **21** and **22** were formed after the perforation step. One of the contacts **22** was connected to the pixel electrode **20**. Thus was obtained a complete NTFT provided on a pixel electrode as shown in FIG. **5**(B).

The TFT thus obtained comprises a crystalline silicon film composed of silicon crystals having grown oriented along a direction parallel to the substrate. Accordingly, the TFT yields high mobility because the carriers move along the crystal boundary of the one-direction oriented single crystals.

EXAMPLE 6

An example of a circuit structure comprising a PTFT and an NTFT in a complementary manner is described. The structure of the present example is applicable to ICs of image sensors, and pixels and peripheral circuits of liquid crystal display devices.

Referring to FIG. **6**, the fabrication process for the present example is described. A 2,000 Å thick silicon oxide film (not shown in the figure) was deposited by sputtering on a glass substrate **11** as a base coating. Then, an amorphous silicon film **12** was deposited thereon by plasma CVD, and was annealed by heating at 600° C. for a duration of 24 hours.

It is extremely favorable to apply annealing using an IR light to the resulting structure after the heating step above for crystallization. The irradiation of an IR light not only eliminates the defects and the dangling bonds in the silicon film, but also improves the crystallinity of silicon and thereby densifies the film. Particularly preferred is the use of a near IR light about 1 to 2 μm in wavelength, because the light in this region is absorbed selectively by the silicon film but not by the glass substrate. Accordingly, the silicon film can be heated to about 800° C. without considerably heating the glass substrate.

Then, two island-like active layers are established by isolating the elements. These two active layers later become a PTFT and an NTFT. A silicou oxide film **13** as a gate insulator film was deposited thereafter at a thickness of 1,500 Å by sputtering. In the same manner as in Example 5, ion implantation for introducing nitrogen ions into the silicon oxide film was carricd out to obtain a silicon oxynitride film **13** as the gate insulator film. The resulting structure is shown in FIG. **6**(B).

Gate contacts **31** and **33** were formed by patterning a 6,000 Å thick aluminum film having formed on the gate insulator film **13**. The surface of the gate contacts **31** and **33** was oxidized by anodic oxidation to form oxide layers **32** and **33** on the surface of the gate contacts. Furthermore, phosphorus ions and boron ions were introduced in turn into corresponding one of the active layer regions respectively after masking it with a resist. In this manner, P-type portions **35** and **37** and N-type portions **38** and **40** can be obtained. Thus were obtained source/drain regions **35** and **37** for the PTFT together with a channel forming region **36** for the PTFT and source/drain regions **38** and **40** for the NTFT together with a channel forming region **39** for the NTFT in a self-aligned manner. A laser beam or IR light is irradiated thereafter to anneal the source/drain regions. The resulting structure is given in FIG. **6**(C).

A polyimide or a silicon oxide film was formed as an interlayer insulator **41**, and electrodes **42**, **43**, and **44** were formed after the perforation step. Thus was realized a complete structure comprising a PTFT and an NTFT whose output are connected with an electrode **43**. Thus was obtained a structure shown in FIG. **6**(D).

As described in the foregoing, the present invention provides a TFT by a low temperature process and at high yield. In particular, the present invention makes a great contribution to the industry when TFTs are formed on a large area substrate to use in active matrices and driver circuits. Though not specifically described in the examples, the present invention may be applied to the fabrication of a so-called three-dimensional IC by superposing semiconductor ICs on single crystal ICs and other types of ICs. Furthermore, though the examples above referred mainly to various types of LCDs, clearly, the present invention is applicable to circuits which are directly formed on an insulator substrate, such as image sensors. Moreover, the use of a silicon oxynitride film as the gate insulator results in the following advantages.

A dense gate insulator can be obtained; this leads to the solution of the problems of fixed charge inside the gate insulator, static breakdown, and pinholes; and The gate insulator can be formed thickly.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof.

What is claimed is:

1. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film and a gate insulator film over a substrate;

forming an interlayer insulator comprising an organic resin over the semiconductor film; and

forming a pixel electrode over the interlayer insulator and electrically connected to the semiconductor film through a wiring,

wherein the wiring includes a first layer and a second layer thereon, said second layer comprising aluminum,

wherein the first layer is in contact with the semiconductor film, and

wherein the pixel electrode is in contact with the first layer.

2. A method according to claim **1**, wherein the pixel electrode comprises indium tin oxide.

3. A method according to claim **1**, wherein the gate insulator film is formed by using an organic silane comprising tetraethoxysilane.

4. A method according to claim **1**, further comprising a step of irradiating the semiconductor film and the gate insulator film with a laser light.

5. A method according to claim **1**, wherein the first layer and the second layer are continuously formed by sputtering.

6. A method according to claim **1**, wherein the organic resin comprises polyimide.

7. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film and a gate insulator film over a substrate;

forming an interlayer insulator comprising an organic resin over the semiconductor film; and

forming a pixel electrode over the interlayer insulator and electrically connected to the semiconductor film through a wiriug,

wherein the wiring includes a first layer and a second layer thereon, said second layer comprising aluminum,

wherein a thickness of the second layer is larger than that of the first layer,

wherein the first layer is in contact with the semiconductor film, and

whercin the pixel electrode is in contact with the first layer.

8. A method according to claim **7**, wherein the pixel electrode comprises indium tin oxide.

9. A method according to claim **7**, wherein the gate insulator film is formed by using an organic silane comprising tetraethoxysilane.

10. A method according to claim **7**, further comprising a step of irradiating the semiconductor film and the gate insulator film with a laser light.

11. A method according to claim **7**, whercin the first layer and the second layer are continuously formed by sputtering.

12. A method according to claim **7**, whereiu the organic resin comprises polyimide.

13. A method for manufacturing a semiconductor device comprisiug the steps of:

forming a semiconductor film and a gate insulator film over a substrate;

forming an interlayer insulator comprising an organic resin over the semiconductor film; and

forming a pixel electrode over the interlayer insulator and electrically connected to the semiconductor film through a wiring,

wherein the wiring includes a first layer comprising chromium and a second layer comprising aluminum thereon,

wherein a thickness of the first layer is 20 to 200 nm and that of the second layer is 100 to 2000 nm,

wherein the first layer is in contact with the semiconductor film, and

wherein the pixel electrode is in contact with the first layer.

14. A method according to claim **13**, wherein the pixel electrode comprises indium tin oxide.

15. A method according to claim **13**, wherein the gate insulator film is formed by using an organic silane comprising tetraethoxysilane.

16. A method according to claim **13**, further comprising a step of irradiating the semiconductor film and the gate insulator film with a laser light.

17. A method according to claim **13**, wherein the first layer and the second layer are continuously formed by sputtering.

18. A method according to claim **13**, wherein the organic resin comprises polyimide.

19. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film and a gate insulator film over a substrate;

forming an interlayer insulator comprising an organic resin over the semiconductor film;

forming a pixel electrode over the interlayer insulator and electrically connected to the semiconductor film through a wiring

wherein the wiring includes a first layer comprising chromium and a second layer comprising aluminum thereon,

wherein the first layer is in contact with the semiconductor film, and

wherein the pixel electrode is in contact with the first layer.

20. A method according to claim **19**, wherein the pixel electrode comprises indium tin oxide.

21. A method according to claim **19**, wherein the gate insulator film is formed by using an organic silane comprising tetraethoxysilane.

22. A method according to claim **19**, further comprising a step of irradiating the semiconductor film and the gate insulator film with a laser light.

23. A method according to claim **19**, wherein the first layer and the second layer are continuously formed by sputtering.

24. A method according to claim **19**, wherein the organic resin comprises polyimide.

25. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film and a gate insulator film over a substrate;

forming an interlayer insulator comprising an organic resin over the semiconductor film;

forming a pixel electrode over the interlayer insulator and electrically connected to the semiconductor film through a wiring,

wherein the wiring includes a first layer comprising chromium and a second layer comprising aluminum thereon,

wherein a thickness of the second layer is larger than that of the first layer,

wherein the first layer is in contact with the semiconductor film, and

wherein the pixel electrode is in contact with the first layer.

26. A method according to claim **25**, wherein the pixel electrode comprises indium tin oxide.

27. A method according to claim **25**, wherein the gate insulator film is formed by using an organic silane comprising tetraethoxysilane.

28. A method according to claim **25**, further comprising a step of irradiating the semiconductor film and the gate insulator film with a laser light.

29. A method according to claim **25**, wherein the first layer and the second layer are continuously formed by sputtering.

30. A method according to claim **25**, wherein the organic resin comprises polyimide.

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